MODELING AND DESIGN OF DEEP-SUBMICRON FULLY DEPLETED SILICON-ON-INSULATOR COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR FOR LOW-VOLTAGE INTEGRATED CIRCUIT APPLICATIONS

BY

PING CHIN YEH

A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

1996

ACKNOWLEDGEMENTS

I would like to express my deep gratitude toward my advisor, Professor Jerry G. Fossum, for his support and encouragement throughout my graduate study. Without his invaluable guidance, this work could not have come to fruition. I also would like to thank Professors R. M. Fox, M. E. Law, T. Nishida, and C. C. Hsu for their willing service and guidance on my committee.

I am grateful to Texas Instruments, Inc., and the Semiconductor Research Corporation for the technical and financial support throughout my research. Especially, I wish to thank Dr. Lisa T. Su for providing measurement data which enhanced the integrity of this work.

I also would like to thank my colleagues, Dr. Dongwook Suh and Mr. Srinath Krishnan, who helped me with the stimulating discussions and technical suggestions. Gratitude is also extended to many of my friends for their help during my graduate study; I would like to mention Messrs. Samir Chaudhry, Tzung Yin Lee, Ming-Yeh Chuang, Dukhyun Chang, Jonathan Brodsky, and Doug Weiser.

My deepest gratitude goes to my parents and parents-in-law for their emotional support. Last, but not the least, I thank my lovely wife, Chia Chih, whose endless love and encouragement were most valuable to me. Without her, the years of my graduate study would have been hard and spiritless.

TABLE OF CONTENTS

page

ACKNOWLEDGEMENTS.....ii

ABSTRACT.....vi

CHAPTERS

1 INTRODUCTION 1

2 ASSESSMENT OF FLOATING-BODY BIPOLAR EFFECTS ON FULLY DEPLETED SOI CMOS CIRCUIT PERFORMANCE 10

2.1 Introduction 10
2.2 Review of FD/SOI MOSFET Model/SOISPICE-2 11
2.3 Problems and Potential Benefits of the Parasitic BJT in Digital Circuit Operation ... 17
2.3.1 Single-Stage CMOS Inverter 19
2.3.2 CMOS SRAM Cell 23
2.4 Benchmark Study of FD/SOI and Bulk-Silicon Technologies 28
2.5 Summary 36

3 A PHYSICAL SUBTHRESHOLD MODEL FOR DEEP-SUBMICRON FULLY DEPLETED SOI MOSFETS 38

3.1 Introduction 38
3.2 Numerical Device Simulations 40
3.3 Subthreshold-Current Model Development 46
3.3.1 Potential Distribution in the SOI Film ... 46
3.3.2 Fringe-Field Analysis in the Underlying Oxide 51
3.3.3 Current Derivation 55
3.4 Modifications of Strong-Inversion Analysis for Including Surface States 59
3.5 Moderate-Inversion Analysis 61
3.5.1 Boundaries of the Moderate-Inversion Region 61
3.5.2 Channel Current 64

3.6 Charge Modeling 65
3.6.1 Intrinsic Weak-Inversion Terminal Charges 66
3.6.2 Intrinsic Moderate-Inversion Terminal Charges 68
3.6.3 Source/Drain Substrate Depletion Charges 69
3.7 Summary 70

4 MODEL IMPLEMENTATION/VERIFICATION 72

4.1 Introduction 72
4.2 Model Implementation in SOI-SPICE-4 73
4.2.1 Model Algorithm 73
4.2.2 Modified Source Code from SOISPICE-2 81
4.3 PISCES/MEDICI Support 84
4.4 Comparison with Device Measurements 90
4.5 Summary 95

5 DESIGN AND PERFORMANCE CONSIDERATIONS FOR SCALED FULLY DEPLETED SOI CMOS IN LOW-VOLTAGE APPLICATIONS 97

5.1 Introduction 97
5.2 Viable Quarter-Micron SOI CMOS Design 98
5.2.1 Preliminary Design 102
5.2.2 n^+ Poly-Gate Alternative 107
5.2.3 Hybrid CMOS Alternative 109
5.3 Design Complications for Highly Scaled FD/SOI 116
5.3.1 Subthreshold Kink Effect 116
5.3.2 Back-Gate Depletion Effect 122
5.4 Optimal Scaling for Deep-Submicron FD/SOI 126
5.5 Summary 133

6 DUAL-GATE FULLY DEPLETED SOI: A PROMISING TECHNOLOGY FOR FUTURE DIGITAL APPLICATIONS 134

6.1 Introduction 134
6.2 DG FD/SOI MOSFET Fabrication 137
6.3 Examination of DG FD/SOI Performance 140
6.3.1 Short-Channel Effect Immunity 140
6.3.2 Threshold Voltage Controllability 144
6.3.3 Current Drive 151
6.4 Preliminary Sub-0.1μm DG FD/SOI CMOS Design ...152
6.5 Summary 153

7 SUMMARY AND SUGGESTIONS FOR FUTURE WORK 156

REFERENCES 161

BIOGRAPHICAL SKETCH 167

Abstract of Dissertation Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy

MODELING AND DESIGN OF DEEP-SUBMICRON FULLY DEPLETED SILICON-ON-INSULATOR COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR FOR LOW-VOLTAGE INTEGRATED CIRCUIT APPLICATIONS

By

Ping Chin Yeh

December 1995

Chairman: Professor Jerry G. Fossum
Major Department: Electrical and Computer Engineering

This dissertation describes physical modeling and design of fully depleted (FD) silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistors (MOSFETs) for low-voltage, deep-submicron complementary-MOS (CMOS) digital integrated circuit (IC) applications. The problematic and possibly beneficial effects of the parasitic bipolar junction transistor (BJT) in scaled FD/SOI CMOS circuits are analyzed using SOI-SPICE, a semi-numerical device/circuit simulator. The study reveals that the bipolar problem, which translates to loss of gate control, overwhelms the benefit, and hence must be alleviated by controlling the activation of the BJT via design tradeoffs. A feasible submicron design approach is demonstrated by veritable device/circuit simulations, which also predict significant speed superiority of SOI over bulk-silicon CMOS circuits, especially for low-voltage applications. As the

channel length is scaled to the deep-submicron regime, the viability of thin-film FD/SOI is threatened by prohibitively low threshold voltage and high off-state current. Our study based on two-dimensional device simulations shows that the off-state current and subthreshold gate swing are governed by gate-bias dependent source/drain charge sharing and fringing fields in the back oxide, which control back-channel as well as front-channel conduction. The insight from this study guides the development of a physical, two-dimensional analytic model for the FD/SOI MOSFET subthreshold current and charge, which is implemented in SOI-SPICE and linked to the strong-inversion formalism to enable predictive scaled device/circuit simulation. The model is verified by two-dimensional numerical simulations and measurements of devices with varying dimensions, the latter being facilitated by a simple parameter-evaluation algorithm defined based on the structural dependences of the physical model parameters. The utility of the enhanced version of SOI-SPICE is demonstrated by using it to define a viable design for deep-submicron (0.2 μm) FD/SOI CMOS technology based on simulated speed and static power in digital circuits. The further scalability of FD/SOI CMOS is then examined using SOI-SPICE. The results are not encouraging however, and indicate a need for significant technology innovation for viable FD/SOI CMOS in the future. Such innovation might render the dual-gate FD/SOI MOSFET practical. SOI-SPICE and numerical device simulations are used in a preliminary assessment of this structure, lending some optimism to the future of FD/SOI technology.

CHAPTER 1
INTRODUCTION

Silicon-On-Insulator (SOI) metal-oxide-semiconductor field-effect transistors (MOSFETs) technology has been known to be superior to bulk-silicon technology in very large-scale integration (VLSI) applications due to easy isolation and simple processing [Col91]. The complete electrical isolation of devices afforded by SOI technology reduces parasitic effects such as junction capacitance and leakage current by minimizing the source/drain junction area. The insulating oxide under the SOI island provides high soft-error immunity, elimination of CMOS latch-up, and reduction of source/drain and first-layer interconnect capacitances because of low dielectric constant. Another advantage of SOI for CMOS is simple processing. For instance, there is no need to create diffusion wells and trench isolation in SOI CMOS circuits since the transistor is completely isolated. This results in an increase in packing density relative to contemporary digital bulk-silicon technology. Furthermore, while forming needed shallow junctions is a major task in scaled bulk-silicon technology, it can be realized in SOI by simply scaling down the film thickness. These advantages render SOI potentially competitive with contemporary bulk silicon as digital IC technology evolves toward deep submicron dimensions.

Fig. 1.1 illustrates the basic structure of an n-channel thin-film SOI MOSFET fabricated using separation by implanted oxygen (SIMOX) [Col91] technology. The channel has a bulk MOSFET-like structure, but is built on a dielectric (oxide) layer instead. We are concerned with modes of operation in which the silicon-film body is fully depleted (FD) because the resultant front gate-back gate charge coupling underlies many potential advantages relative to the partially depleted (PD) device [Fos93], for example, immunity to the floating-body kink effect, nearly ideal subthreshold slope, enhanced current drivability, and reduced short-channel effect. Recently it was also found that FD operation exhibits no dynamic floating-body effect as the PD device does in transient circuit operation [Tsu94].

There is a major interest in developing SOI technology for low-voltage/low-power applications such as battery-operated portable information systems. In this field FD/SOI can provide superior speed and low power consumption because of the ideal subthreshold characteristics and scalable threshold voltage afforded by the variable (thin) silicon film. Furthermore, unlike the bulk-silicon junction capacitance, the source/drain capacitance of SOI does not increase with lowering supply voltage, and is always less than that of the bulk device, especially at low voltage. The reduced parasitic capacitance is a key issue in enhancing the circuit performance in low-voltage operation. Various circuits utilizing deep-submicron FD/SOI technology have been fabricated showing the expected superior performance.

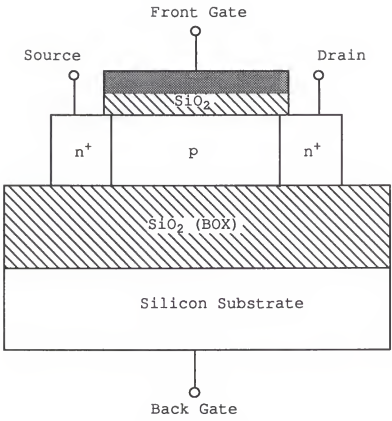


Fig. 1.1 A cross-sectional view of an n-channel FD/SOI MOSFET

For example, Tsu et al. showed that at a supply voltage of 1.2 V, a LSI phase-lock loop (PLL) fabricated using 0.24-μm CMOS/SIMOX technology can operate at 1 GHZ with only 1 mW of power consumption, which is less than 1/10 that of a recently reported bulk-silicon BICMOS circuit operating at about the same speed [Tsu94]. Kado et al. fabricated a 0.25-μm-gate ultra-thin-film CMOS SIMOX gate array. They showed that the total power of loaded CMOS/SIMOX logic gates is 3-4 times smaller than that of 0.35-μm bulk CMOS gates, and obtained 30-40% speed improvement [Kad95].

However, there are still some potential problems that need to be examined before a broad commitment to FD/SOI technology can be made. For instance, to realize the packing advantage afforded by simple isolation in SOI, the body of the MOSFET is normally left floating. This creates floating-body problems, the most annoying of which is the activation of the parasitic bipolar transistor which causes the device to latch and produce significant standby current [Cho91]. In addition, as the device dimension is shrunk to the deep-submicron region for increasing circuit density, the subthreshold ideality in FD/SOI tends to deteriorate due to the two-dimensional field in the film body and buried oxide. This increases the static power consumption. There is concern also about the sensitivity of threshold voltage to the film thickness since the film must be very thin to assure the FD condition and improve the short-channel effects.

To study whether these problems can be tolerated or can be optimized, and to exploit the unique benefits afforded by thin-film SOI technology, we need a reliable and physical

device/circuit simulator. SOISPICE-2 [Fos92], an enhanced version of SPICE-2G [Nag75], has been the most reliable SOI circuit simulator available to industry. The implemented FD MOSFET model developed by Lim [Lim85], Veeraraghavan [Vee89], and Choi [Cho91] physically account for most unique features of the thin-film SOI MOSFET. These include, to name a few, front gate-back gate charge coupling [Lim85], short-channel effects (e.g., source/drain charge sharing, drain-induced barrier lowering, drain-induced current enhancement, channel length modulation) [Vee89], parasitic BJT effects [Cho91], and subthreshold currents for both front and back surfaces [Cho91]. These models make SOI-SPICE a useful aid for submicron SOI CMOS technology and circuit design.

Meanwhile, CMOS technology has reached sub-0.5μm, or deep-submicron feature size, and future scaled generations are being developed for low supply voltage to reduce power consumption while maintaining reliable operation. Lowering the supply voltage requires reducing the threshold voltage for speed retention, which tends to increase leakage current. Robust yet compact subthreshold modeling is therefore desirable for assessing and optimizing SOI CMOS design with regard to circuit speed and power dissipation. While the previously developed SOI-SPICE MOSFET model is useful for simulating submicron FD/SOI circuit speed performance, the weak-inversion modeling is inadequate for predicting the subthreshold characteristics of deep-submicron devices. The model simplifies the effects of the complex two-dimensional electric field in the film and

(thick) back-gate oxide, which in fact influence the device's subthreshold characteristics significantly.

The purpose of this dissertation, then, is to develop an accurate subthreshold current/charge model with afforded physical insights, and to conduct comprehensive simulation studies for optimization of FD/SOI CMOS performance in deep-submicron low-voltage digital IC applications. The major contributions made in this dissertation are:

(1) assessment of the problematic and possible beneficial effects of parasitic BJT in scaled FD/SOI CMOS circuits, and suggestion of viable design approach;

(2) development of a physical subthreshold current/charge model to accurately predict the device subthreshold characteristics for different channel lengths as well as the other structural parameters;

(3) implementation of the developed model in SOI-SPICE to create "SOI-SPICE-4", which is a useful simulation aid for deep-submicron SOI CMOS technology and circuit design, especially for low supply voltage where a good tradeoff between increasing speed and reducing power dissipation is the major concern;

(4) identification of viable designs for deep-submicron (0.2 μm) low-voltage FD/SOI CMOS technology, and examination of its scalability as well;

(5) preliminary assessment of the performance of the dual-gate FD/SOI MOSFET for future FD/SOI technology.

In Chapter 2, we review a previously developed physical model [Cho91] for the FD/SOI MOSFET, and use it to assess the performance of submicron SOI CMOS digital circuits.

Representative device and circuit simulations reveal prohibitive standby-current and possible erroneous-function problems caused by activation of parasitic BJT in the scaled FD/SOI CMOS circuit. The simulations suggest that optimally designed LDD and LDS regions can effect a good tradeoff between alleviating the BJT-induced problems and reducing current drive. Ring-oscillator simulations, in accord with measurements, further predict significant speed superiority of fully depleted SOI over bulk-silicon CMOS circuits in scaled, submicron technologies. The simulations also provide the insight needed to explain this superiority of SOI over bulk technology.

The advantages of SOI over bulk-silicon CMOS, such as ideal subthreshold slope (or gate swing S) and low leakage current, seem to disappear when the channel length is scaled to the deep-submicron regime. In Chapter 3, our two-dimensional numerical device simulations, in accord with published measurements, reveal that the S ideality tends to be sacrificed and in fact preempted by prohibitively low threshold voltage and high leakage current. Our study shows that the front-surface current contributes to the increased S via gate bias-dependent source/drain charge sharing. The current throughout the SOI film body, including the back surface, also tends to overwhelm the front-surface current and increases S even more. Based on the physical insights gained from the numerical device simulations, we derive a two-dimensional analytic solution for the potential, accounting for the fringe-field effect at the back surface. We also model the diffusion of carriers throughout the film

body, and account for (front and back) channel-length modulation. A cubic spline is used to link the derived model to the previously developed short-channel FD/SOI MOSFET model [Vee88]. This interpolation thus effectively accounts for the moderate-inversion region of the simulated device, and thereby gives a rigorous look at threshold voltage and its dependence on device structure.

In Chapter 4, the model implementation into the SOI-SPICE circuit simulator is described in detail. A model hierarchy is structured to give the user flexibility in choosing different levels of the FD/SOI model for circuit simulations. Thorough model verifications with numerical device simulations and experimental data are also presented.

In Chapter 5, we use SOI-SPICE to examine how all the vertical dimensions (front and back oxide thickness, as well as film thickness) and the body doping can be scaled with the channel length to yield a viable FD/SOI CMOS design for deep-submicron (0.2 μm) low-voltage applications. Various design alternatives are identified and checked based on simulated speed and static power consumption, and the scaling capability of FD/SOI CMOS is assessed at the device/circuit level.

In Chapter 6, SOI-SPICE is used to gain physical insight and to check the performance of the dual-gate FD/SOI MOSFET with regard to immunity to the short-channel effect and control of the threshold voltage. Comparisons with the performance of conventional FD/SOI CMOS in the sub-0.1μm regime imply some optimism for the novel device structure in future FD/SOI technology.

In Chapter 7, we summarize the main accomplishments of this work and suggest some future work.

CHAPTER 2
ASSESSMENT OF FLOATING-BODY BIPOLAR EFFECTS ON FULLY DEPLETED SOI CMOS CIRCUIT PERFORMANCE

2.1 Introduction

Fully depleted (FD) SOI CMOS is potentially competitive in VLSI applications because of eased scaling afforded by the variable (thin) silicon film thickness as well as simple isolation [Col91]. The viability of SOI however is threatened by floating-body problems, the most annoying of which for FD/SOI is due to the impact ionization-triggered activation of the parasitic (npn) bipolar junction transistor (BJT) in the (n-channel) SOI MOSFET structure [Cho91]. This effect, which results in loss of gate control, has been extensively analyzed at the device level under dc conditions (i.e., by examining source-drain breakdown and subthreshold conduction), but little study of the effect and its repercussions has been done at the circuit level under transient conditions. Furthermore, little study of the possible benefit to circuit speed afforded by the BJT activation has been done.

In this chapter, we will first review a physical model for the fully depleted SOI MOSFET, written into SPICE2 source code, and then use it to assess the performance of submicron FD/SOI CMOS digital circuits. The BJT-induced problems are found to overwhelm the benefits, and a feasible

approach to the design tradeoff needed to inhibit them is demonstrated by device/circuit simulations. Ring-oscillator simulations, in accord with measurements, still predict significant speed superiority of FD/SOI over bulk-silicon CMOS circuits in scaled, submicron technologies. The simulations also provide the insight needed to explain this superiority of SOI.

2.2 Review of FD/SOI MOSFET Model/SOISPICE-2

The FD/SOI MOSFET model in SOISPICE-2 [Fos92] is a major extension of the previously developed short-channel, charge-based model [Vee88] for the thin-film SOI MOSFET. The noteworthy extensions [Cho91] are accountings for subthreshold current at both the front and back surfaces, for lightly doped drain (LDD) and lightly doped source (LDS) regions, as well as for the impact-ionization currents and the parasitic BJT in the LDD/LDS device structure shown in Fig. 2.1. The new five-terminal (source, drain, front gate, back gate, and body) model, represented in Fig. 2.2, is based on the assumption of a fully depleted film body. The analyses of the (ambipolar) carrier transport in the device structure which underlies the model require iterative, Newton-like numerical solution, mainly because of the LDD analysis which must be physically linked to the channel and BJT analyses. The model algorithm is hence semi-numerical, yet is implemented effectively in SPICE2 source code creating "SOISPICE-2" [Cho91], which enables reliable and efficient mixed-mode device/circuit simulation.

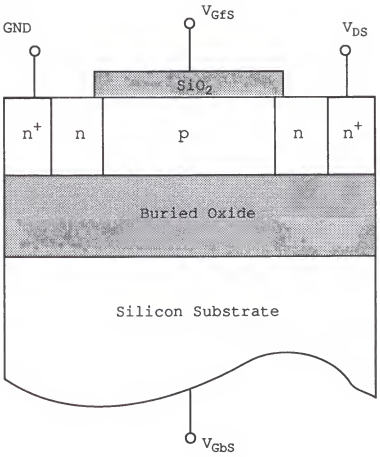


Fig. 2.1 Cross-sectional view of the contemporary thin-film SOI MOSFET including an LDD and LDS.

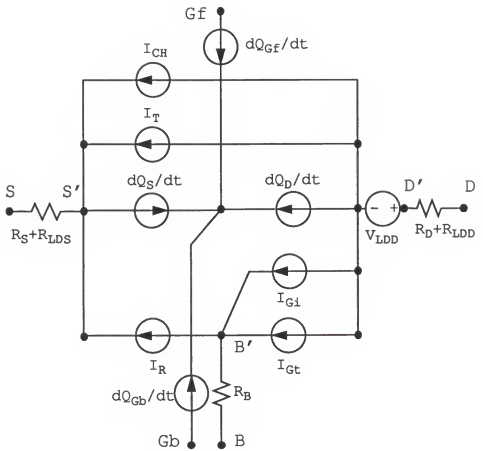


Fig. 2.2 Network representation of the five-terminals, charge-based FD/SOI MOSFET model.

The subthreshold channel currents are modeled as weak-inversion current, constrained by V_{DS}-dependent limits and added to the strong-inversion current in [Vee88]. The basic weak-inversion current expression, applied to both front and back channels, is formulated to be consistent with the physical characterizations of short-channel and gate charge-coupling effects in [Vee88].

The new modeling of the impact ionization and the parasitic BJT is especially important with regard to our study of the bipolar effect in SOI CMOS IC. The characterization of the (weak) impact-ionization current I_{Gi} extends that in [Vee88] by accounting for carrier generation in the LDD as well as the high-field portion of the channel (where the electron velocity is assumed to be saturated), and by including the BJT transport current I_T and the total (front- and back-) channel current I_{CH} in the driving electron current:

$$I_{Gi} = (M-1)(I_{CH} + I_T) \tag{2.1}$$

where

$$(M-1) = \int_{L_e}^{L} \alpha_0 \exp\left(-\frac{\beta_0}{|E_y|}\right) dy + \int_{L}^{L+L_{DD}} \alpha_0 \exp\left(-\frac{\beta_0}{|E_y|}\right) dy \ . \tag{2.2}$$

The first integral in (2.2), with L_e defined as the modulated channel length and L as the effective (actual) channel length, follows from [Vee88], but with longitudinal field $E_y(y)$ reduced because of the voltage drop V_{LDD} across the LDD. The second integral in (2.2) depends on $E_y(y)$ in the LDD

derived from Poisson's equation to be consistent with the peak electric field characterized by the channel analysis.

The use of the one-dimensional local-field model for the impact-ionization rate in (2.2) however is possibly deficient for two reasons. First, the electron flow in the device is actually two-dimensional, and second, the impact ionization is actually a nonlocal effect [Slo91]. In fact with regard to the latter, recent work [Slo91] treating the true dependence of impact ionization on carrier energy, which typically lags the electric field, has suggested that the local-field characterization of I_{Gi} (and of associated hot-electron effects) may overly estimate it. Nonetheless, we can still have a reasonable characterization of I_{Gi} using the local-field model provided the impact-ionization coefficients are evaluated by fitting predicted currents to measured ones, which we have done.

The BJT electron transport current is approximated for short L via the classical integral charge-control relation [Mul86]:

$$I_T \cong \frac{qWt_b n_i^2 D_n}{\int_0^{L_{ef}} p\,dy}\left[\exp\left(\frac{qV_{BS}}{KT}\right)-1\right] \tag{2.3}$$

where the effective front-channel length L_{ef} is used as the base width; W is the channel width, t_b is the SOI film thickness, D_n is the average electron diffusivity, V_{BS} is the (induced) body-source forward bias, and

$$\int_0^{L_{ef}} p\,dy \cong \frac{L_{ef} n_i}{2}\exp\left(\frac{qV_{BS}}{2kT}\right)+L_{ef}N_A \tag{2.4}$$

is the integrated hole density with N_A the (uniform) body doping density. The basis for (2.4) is an assumed linear distribution of holes across the (modulated) channel region with $p \cong n > N_A$ in the normally depleted body. Numerical device simulations [Cho91] support this assumption for normal activation of the BJT. That last term in (2.4) is included to keep the model tractable when the device is off and the assumption is not applicable. Numerical device simulations further show that when the parasitic BJT is activated in the FD/SOI MOSFET structure, the primary recombination current I_R (i.e.,injected hole removal current) is supported by the quasi-neutral source region, including the LDS. Thus we have

$$I_R \cong I_{R0}\left[\exp\left(\frac{qV_{BS}}{kT}\right) - 1\right] \tag{2.5}$$

where I_{R0} depends on both structural and electrical parameters of the source region, as well as the ohmic drop (caused by the electron current) in the LDS region [Cho91].

SOISPICE-2 is structured to allow user options in the model. For example, the BJT can be turned off by not including a device-line flag parameter, and the LDD or LDS region can be eliminated by specifying the respective length parameter as zero on the model line. These options allow us to examine the effects of the parasitic BJT and LDD/LDS on the CMOS circuit performance.

2.3 Problems and Potential Benefits of the Parasitic BJT in Digital Circuit Operation

To realize the packing advantage afforded by the simple isolation in SOI, the body is normally left floating, or is intrinsically tied to the source region, which tends to create a virtually floating body because of the high body-source resistance. However, the floating body enables the parasitic bipolar effects. In the n-channel FD/SOI MOSFET, holes generated by channel current-induced impact ionization, or by other generation mechanisms (e.g., thermal generation) near the drain, are injected into the body, causing a forward bias (quasi-Fermi level separation) on the body-source junction. This bias activates the parasitic (lateral) BJT, which injects electrons from the source into the body where they are transported to the drain. This electron current drives additional impact ionization, and the process can become regenerative, resulting in loss of gate control.

As noted in [Cho91], the activation of the BJT can be suppressed by using a properly designed LDS to enhance the source recombination and reduce the bipolar gain (I_T/I_R). However, the need for an LDD to limit (M-1) as indicated in (2.2), as well as to control other detrimental hot-electron effects, implies for technological reasons the inclusion of the identical LDS, which hence must be designed in accord with design criteria for the LDD. Relevant insight is provided by SOISPICE-2-simulated current-voltage characteristics in Fig. 2.3 of a 0.5-μm n-channel FD/SOI MOSFET in a 100-nm-thick film. Without LDD and LDS, the

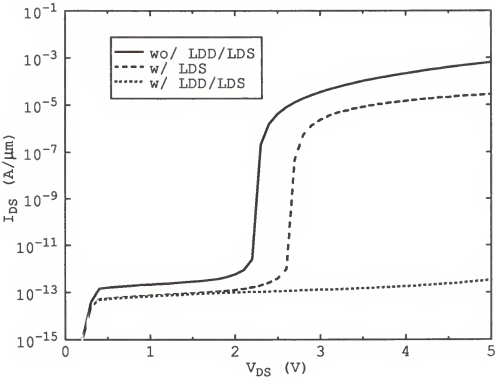


Fig. 2.3 Simulated off-state latch characteristics of an L = 0.5 μm SOI MOSFET with and without LDD/LDS at V_{GfS} = 0.

device is latched at V_{DS} = 2.2 V, resulting in significant leakage current. The predicted benefits of an LDD and LDS, doped in this example at 10^{17} cm^{-3} with length of 0.2 μm, in controlling the BJT-induced off-state latch are also apparent.

Obviously, optimally designed LDD and LDS regions can effectively suppress the BJT-induced problems. There is however a tradeoff involved because of the voltage drops across these regions and the concomitant reduced drive-current capability of the MOSFET. To rigorously assess the viability of fully depleted SOI CMOS VLSI, the effects of the parasitic BJT as induced by actual circuit operation and the performance tradeoffs involving the LDD/LDS structure must be studied at the circuit level under transient conditions.

2.3.1 Single-Stage CMOS Inverter

Consider initially the simple SOI CMOS inverter. It is obvious that in the output-high steady state, if the supply voltage (V_{DD}) is greater than the BJT-defined off-state latch voltage, the n-channel transistor will latch, causing excessive standby current. The high-state voltage is thus lowered and, depending on the conductance of p-channel transistor, the inverter can lose functionality if the holding voltage (Fig. 2.3) is extremely low. Such failure is indeed a tendency in deep-submicron devices as implied by (2.3) and (2.4). This condition can also be induced by the pull-up transient if V_{DD} is greater than the holding voltage.

During the pull-down transient, the n-channel transistor can latch provided the rise time of the input voltage pulse is sufficiently short. In this case, channel current is quickly turned on, producing enough impact ionization when the output voltage is still high to activate the parasitic BJT. This on-state latch tends to reduce the pull-down delay because of the supplemental BJT current which facilitates discharging of the load. This latch is not sustained in the steady state because V_{DS} is pulled down to zero, precluding any continued impact ionization. SOISPICE-2 simulations of this transient, for varying fan-out (or load capacitance) with and without the BJT activation, reveal however that the speed benefit is only modest.

In Fig. 2.4, predicted pull-down delays for V_{DD} = 5 V are plotted versus the fan-out. The inverter comprises 0.5-μm transistors with fully depleted, floating bodies in 100-nm film. The n-channel and p-channel gate areas used in the simulations are 0.5×5.0 μm^2 and 0.5×10.0 μm^2, respectively, and the front oxide thicknesses are 15 nm. The simulated n-channel current-voltage characteristics plotted in Fig. 2.5, with and without the BJT activation, show the enhanced current drive (especially at low V_{Gfs}) due to the parasitic BJT. (We ignore the BJT activation in the p-channel device because of the presumed low impact-ionization coefficients for holes.) However, as evident in Fig. 2.4, the BJT-produced speedup is less than 25% in transient operation even for high fan-out. The benefit is minimal mainly because the transient V_{DS} on the MOSFETs during the pull-down quickly drops below the (V_{Gfs}-dependent) holding voltage, thereby

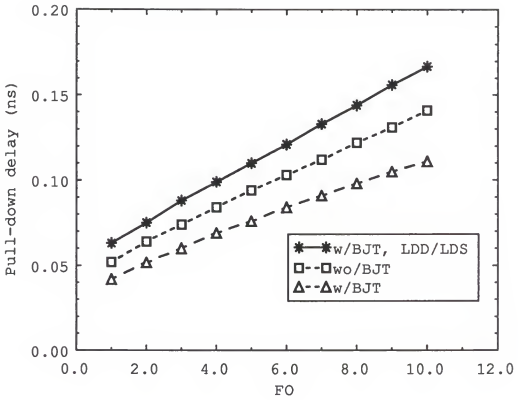


Fig. 2.4 SOISPICE-2-predicted pull-down delays of SOI CMOS inverter versus fan-out (FO = 1 is equivalent to a 0.0094-pF load), with and without parasitic BJT activation, and with and without LDD/LDS to inhibit BJT.

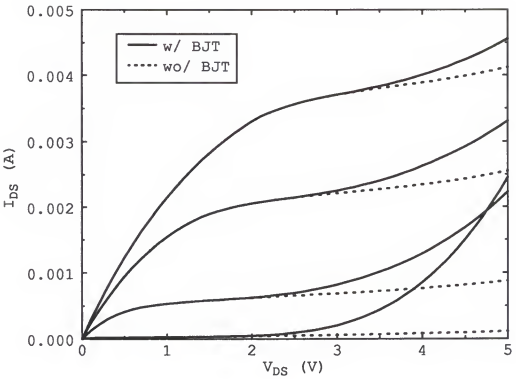


Fig. 2.5 Simulated drain current-voltage characteristics (V_{GfS} = 0, 1, 3, 5 V) for the n-channel MOSFET used in Fig. 2.4, showing the enhanced current drive capability in DC condition due to the parasitic bipolar activation. The holding voltage for this device is about 2.3 V (at V_{GfS} = 0).

deactivating the BJT for most of the transient. The predicted $I_{DS}(t)$ characteristics, with and without the BJT activation, shown in Fig. 2.6 further confirm this explanation. Also noted in Fig. 2.6 is the prohibitive standby current (caused by off-state latch) before the transistor is turned on. Thus we conclude that the floating-body BJT effect is not beneficial, while the standby-current problem appears to be the predominant issue in design optimization.

Also included in Fig. 2.4 are the corresponding delays predicted when an LDD and LDS, both doped at 3×10^{17} cm^{-3} and of length 0.2 μm, are used to inhibit the BJT. Note that these delays are somewhat longer because of the LDD/LDS voltage drops, indicating a critical, but seemingly doable design tradeoff. The delays predicted by SOISPICE-2, even with suboptimal LDD/LDS as in Fig. 2.4, are shorter than those of the bulk-silicon CMOS counterpart near the L = 0.5 μm scaling level [Yam89].

2.3.2 CMOS SRAM Cell

Consider now the basic six-transistor SOI CMOS SRAM cell shown in Fig. 2.7, in which the aforementioned effects as well as other unique transient effects can occur due to the floating, fully depleted body. In steady states, the off-state latch can obtain in any of the four n-channel transistors, producing prohibitive standby current in the memory element and/or in the access lines. Furthermore, transient-induced latches and upsets can occur because of

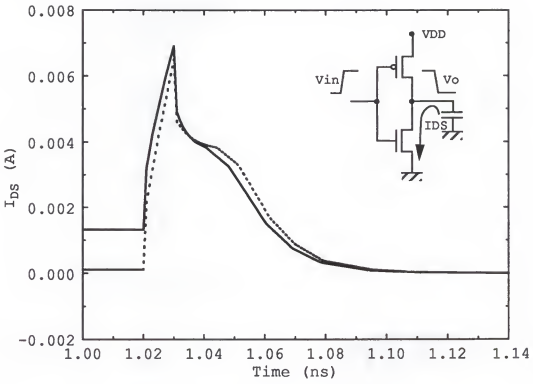


Fig. 2.6 Simulated pull-down transient current of the n-channel SOI MOSFET with (solid curve) and without (dot curve) BJT activation. The rise time of the input pulse is 10 ps.

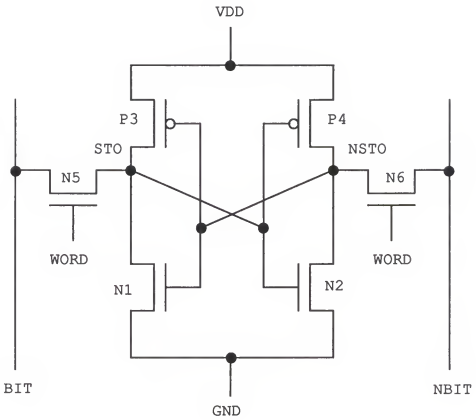


Fig. 2.7 (SOI) CMOS SRAM cell

the BJT, producing some speed-up as well as standby currents. Consider a write operation, for example writing a "1" (on the drain of N1). The pertinent node-voltage and current transients, obtained from SOISPICE-2 simulations with the parasitic BJT activated, are plotted in Fig. 2.8. The transistor gate areas used in the simulations are representative of advanced SOI CMOS technology with L = 0.5 μm. Prior to the gate activation of the access transistors, the high logic level (on the drain of N2) is reduced because of the off-state latch of N2. The initial transient then results in the latching of the access transistors N5 and N6, tending to speed up the write operation. As for the inverter, this speed enhancement is modest; the write-"1" delay in Fig. 2.8 is 0.23 ns, which is only about 25% less than the delay predicted when the BJTs are not activated. When the "1" is written, N5 and N6 are no longer latched, but N1 is latched, keeping the logic level below V_{DD} because of the standby current. If the conductivity of the p-channel load transistor is too low and the holding voltage of the n-channel drive transistor is only a small fraction of V_{DD}, it is impossible to write a logic "1" in the cell. The deactivation pulses finally cause the access transistors N5 and N6 to latch again, resulting in further distortion of the logic levels because of standby current flowing in all the transistors. Clearly the BJT-induced standby currents in the cell are prohibitive, whereas the speed benefit is not significant.

The effects occurring in a read operation are somewhat different. Consider first reading a "0" (on the drain of N1)

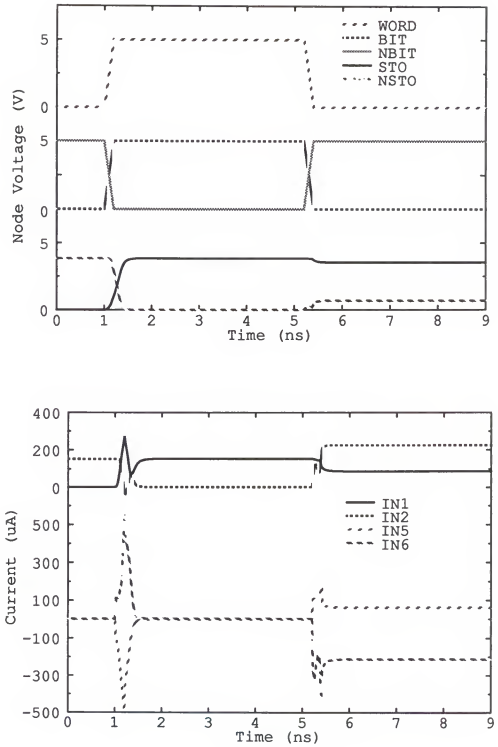


Fig. 2.8 Node-voltage and current transients from SOISPICE-2 simulation of write-"1" operation in SOI CMOS SRAM cell with BJT activations.

with the bit lines capacitively precharged (to V_{DD}). Prior to the gate activation of the access transistors N5 and N6, N5 can be latched, thereby enabling the discharging of the precharge capacitor on the bit line. This is illustrated in Fig 2.9, which shows SOISPICE-2 simulation results with and without the BJT activated. Note that with the BJTs, the precharge on the bit line coupled to the drain of N1 (and realistically to other storage nodes in the memory array) drops, approaching the holding voltage of N5. Nonetheless the read-"0" operation is done properly, and apparently much faster than without the BJT effects. This speed enhancement is however only an artifact of the BJT-induced source-drain coupling in N5. Consider now reading a "1" in an adjacent cell, with the reduced precharge on the bit lines. The SOISPICE-2 simulation results of this operation show that the net result of the BJT activations in this case is an added delay of the access at best and a general inability to unequivocally read the "1" at worst. This disabling is prohibitive, whereas the apparent speed benefit provided by the BJT to the read-"0" operation is inconsequential.

2.4 Benchmark Study of FD/SOI and Bulk-Silicon Technologies

To further demonstrate the viability of using the LDD/LDS to effect a good tradeoff between inhibiting the parasitic bipolar effects and reducing the drive-current capability of the FD/SOI MOSFET, and to benchmark SOI against bulk-silicon CMOS VLSI, we present in Fig. 2.10 results of unloaded nine-stage CMOS ring oscillator

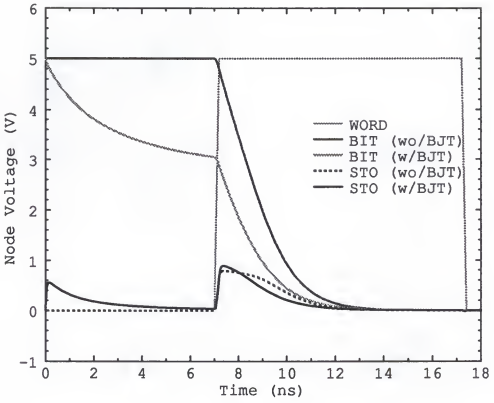


Fig.2.9 Node-voltage transients from SOISPICE-2 simulations of read-"0" operation in SOI CMOS SRAM cell with and without BJT activation.

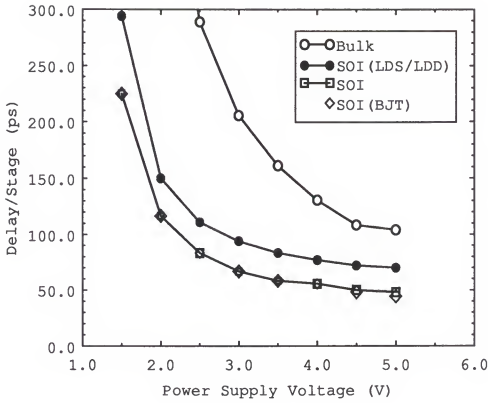


Fig. 2.10 Predicted propagation delay/stage from SOISPICE-2 simulations of nine-stage CMOS ring oscillator showing speed superiority of SOI over bulk silicon for L_{eff} = 0.5 μm technologies.

simulations done with SOISPICE-2. (The first stage is a NAND gate for triggering the oscillation.) Plotted in figure versus the supply voltage V_{DD} are stage propagation delays (calculated from the predicted frequencies of oscillation) for SOI CMOS (with and without the BJT activation, and with LDD/LDS to inhibit the BJT) compared with delays for equal-area bulk-silicon CMOS. The simulations of the latter were done with SPICE2/Level-2 MOSFET models fitted to an actual 0.8-μm technology [Vee90] with 0.5-μm effective channel length. The SOI CMOS simulations were done using physically representative model parameters, with L = 0.5 μm, t_b = 100 nm, t_{of} = 15 nm equal to the gate oxide thickness of the bulk-silicon technology, and t_{ob} = 400 nm. The SOI MOSFET flatband voltages were assigned values to yield threshold voltages (from simulated linear-region current-voltage characteristics) matched to those of the bulk-silicon devices. The source and drain series resistances are matched also. The electric field-dependent carrier mobilities in the SOI MOSFET model were evaluated based on an actual technology [Cho91].

The simulation results in Fig. 2.10 are quite interesting. Note first that although the simulated holding voltage of the n-channel SOI MOSFET is less than 3 V, the parasitic BJT produces only a small speed enhancement at VDD = 5 V, consistent with our findings from the inverter and SRAM-cell simulations. Note next that without the LDD/LDS, the predicted SOI stage delay is less than half that of bulk silicon at V_{DD} = 5 V, and the SOI speed superiority is improved as V_{DD} is scaled down. Indeed this substantive

superiority of fully depleted SOI predicted by SOISPICE-2 is in general accord with corresponding measurements [Woe89] of submicron SOI CMOS ring oscillators. However, to avoid the prohibitive problems caused by the parasitic BJT, some of the speed superiority may have to be sacrificed in a design tradeoff, even though V_{DD} is scaled with L in deep-submicron technologies to limit hot-carrier effects. We use the LDD/LDS structure to effect this tradeoff, with non-optimized parameters: $N_{LDS} = 3 \times 10^{17}$ cm^{-3} and $L_{LDS} = 0.2$ μm. The SOISPICE-2 simulation results for this case in Fig. 2.10 still show a significant speed advantage for SOI CMOS; the predicted SOI stage delay at $V_{DD} = 5$ V is less than 70% of the bulk-silicon delay, with the superiority also improved as V_{DD} is reduced.

Parametric studies based on ring oscillator simulations (without the LDD/LDS) reveal that the significant speed superiority of SOI over bulk-silicon CMOS is due to i) the eliminated source and drain junction capacitances in the SOI structure, which accounts for about 60% of the speedup (note that the bulk perimeter-junction capacitance is not included in the simulations), and ii) the enhanced current drive afforded by the SOI MOSFET because of the inherent higher carrier mobilities and the restricted depletion charge in the body [Col91] [Vee89], which accounts for the other 40%. With regard to ii), we show in Fig. 2.11 simulated current-voltage characteristics of the SOI and bulk-silicon devices. The enhancement in $I_{DS(sat)}$ afforded by the fully depleted SOI, which varies with gate bias because of dependences on carrier mobility and saturated drift velocity [Vee89], is about 50% and 40% for the n-channel and p-channel devices,

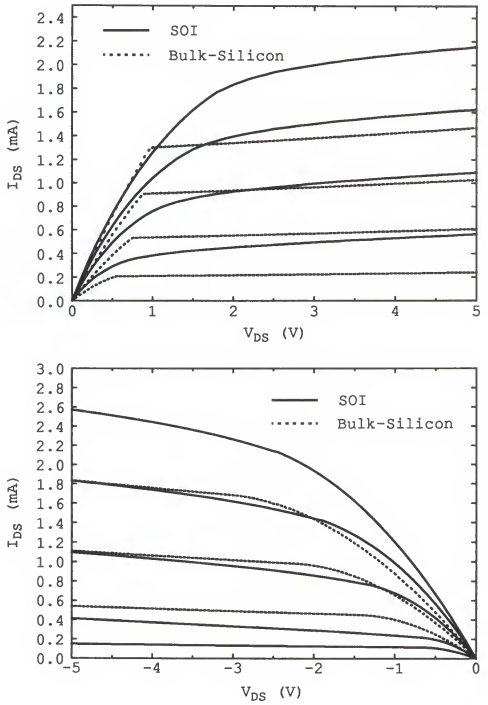


Fig. 2.11 Simulated drain current-voltage characteristics ($|V_{Gfs}|$ = 2, 3, 4, 5 V) for n- and p-channel MOSFETs showing the enhanced drive capability of fully depleted SOI relative to bulk silicon (L = 0.5 μm).

respectively, for gate bias V_{GfS} near 5 V. To ascertain the impact of this enhancement on the ring-oscillator speed, we lowered the carrier mobilities on the SOI devices such that $I_{DS(sat)}$ was reduced to that of the bulk-silicon devices at $V_{GfS} = V_{DD}$, and then simulated the ring oscillator (without the BJT and the LDD/LDS). The predicted SOI stage propagation delay increased from less than 50% to about 70% of the bulk-silicon delay for $V_{DD} = 5$ V.

With regard to i), we simulated the bulk-silicon ring oscillator for decreasing source- and drain- junction areas in Fig. 2.12. Indeed, when these areas approached zero, the predicted stage delay approached that of the modified SOI ring oscillator containing transistors with equal $I_{DS(sat)}$ as described above. This parametric study hence shows that for the assumed L = 0.5 μm technologies, the speed superiority of SOI over bulk-silicon CMOS is due mainly and about equally to reduced source- and drain-junction capacitance and enhanced drive current. Note that in Fig. 2.10 that this speed superiority becomes more pronounced as V_{DD} is scaled. This relative improvement is a natural characteristic of scaled CMOS having inherently less parasitic capacitance, with the junction capacitance of bulk devices having approximately $1/V_{DD}^{0.5}$ dependence due to the source/drain depletion, and higher drive capability. The predicted speed superiority, especially at reduced V_{DD} with the BJT inhibited (about 70% faster at $V_{DD} = 3.3$ V), attests to the viability of SOI and portends a real advantage of SOI over bulk-silicon CMOS for deep-submicron, high-performance design rules, at which punchthrough and the lack of scaling flexibility could

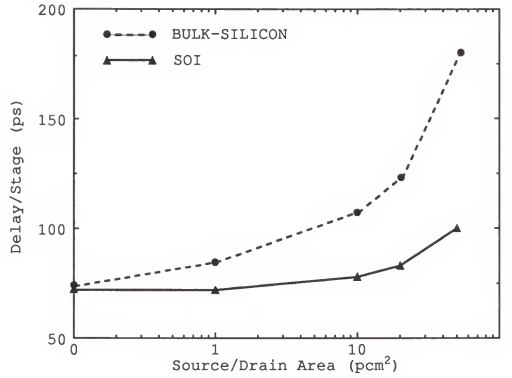


Fig. 2.12 Simulated delay/stage versus source/drain junction area for SOI and bulk technologies.

render the bulk-technology not only inferior to SOI but indeed prohibitive.

2.5 Summary

In this chapter, SOISPICE-2, a version of SPICE2 enhanced with a physical model for the fully depleted SOI MOSFET, was described and used to assess the viability of SOI for submicron CMOS digital circuit applications. Representative circuit simulations revealed prohibitive standby current and possible erroneous-function problems caused by activation of parasitic BJT in the n-channel device structure. The possible benefits, for example, enhanced speed, afforded by the supplemental BJT current, were found to be only modest, and rendered inconsequential by the overwhelming standby-current and functionality problems in actual circuit environments. The BJT effect must be constrained to render a viable technology. SOISPICE-2 simulations suggested that an optimal designed LDD/LDS device structure could effect a good tradeoff between alleviating the BJT problems and reducing drive-current capability. This design tradeoff for viable SOI CMOS VLSI seems doable, partly because of the enhanced drive current as well as the reduced parasitic (junction) capacitance in the device structure. Veritable ring oscillator simulations corroborated this surmise for L = 0.5 μm by predicting a significant speed superiority of SOI over bulk-silicon CMOS, even when a LDD/LDS structure was used to inhibit the BJT and especially for scaled supply voltage. This latter prediction

portends a displacement by fully depleted SOI of the bulk technology, which because of punchthrough and the lack of scaling flexibility could become prohibitive for deep-submicron, high-performance design rules. However characteristics of deep-submicron FD/SOI devices and circuits must be studied to give this notion credence.

CHAPTER 3
A PHYSICAL SUBTHRESHOLD MODEL FOR DEEP-SUBMICRON FULLY DEPLETED SOI MOSFETS

3.1 Introduction

Interest in SOI today is focused mainly on low-voltage/ low-power digital circuits. The nearly ideal subthreshold gate swing (S) of thin-film fully depleted (FD) SOI MOSFETs enables, in principle, reduction of the threshold voltage for speed retention in these applications, without excessive increase in static power. However, in deep-submicron FD devices, the S ideality tends to be sacrificed [Omu93] and in fact preempted by prohibitively low threshold voltage and high off-state current. Several analyses of the physics underlying this deterioration have been done at the device level [You89] [Guo93], but no attention has been paid to modeling the subthreshold current, which is essential for circuit simulation and design optimization of the deep-submicron FD/SOI CMOS technology. While the SOI-SPICE model reviewed in Chapter 2 [Cho91] is useful for simulating FD/ SOI circuit speed performance, it is inadequate for predicting subthreshold leakage current of deep-submicron devices since it overly simplifies the two-dimensional nature of the underlying physics.

In this chapter, a study of the subthreshold characteristics of deep-submicron FD/SOI MOSFETs, based on

two-dimensional numerical device simulations, is described, and insight attained is used to aid the development of a model for circuit simulation. The device simulation results show that the front-surface current contributes to the increase of S via gate bias-dependent source/drain charge sharing, which induces nonuniform fields along the front-gate oxide/silicon interface and reduces the threshold voltage. The study further shows that S is commonly affected by current along the back surface of the SOI film, which is influenced (enhanced) by the two-dimensional field in the underlying oxide; hence the source-drain current is rendered less dependent on the front-gate bias, and S increases even more.

In order to model the subthreshold characteristics properly for low-voltage circuit design, we derive a two-dimensional analytic solution for the potential in the SOI device structure by assuming that the film body is strongly depleted of holes. We account for the weak-inversion diffusion of carriers throughout the thin-film body based on the derived potential solution, which is supplemented with the related charge modeling. We also physically model the bias-dependent substrate depletion charge under the source and drain regions, which is essential in scaled-box design. A cubic polynomial interpolation is used to link the weak- and strong-inversion [Vee88] currents to provide a smooth transition from subthreshold to suprathreshold operation. This interpolation thus effectively accounts for the moderate-inversion region, and thereby gives a rigorous look at the threshold voltage and its dependence on device

structure. The mentioned models are implemented in the SOI-SPICE circuit simulator; the details of implementation and model verification are presented in Chapter 4.

3.2 Numerical Device Simulations

To gain insight concerning the physics underlying the subthreshold conduction in the deep-submicron FD/SOI MOSFET, we used PISCES [Tma89] for two-dimensional numerical simulations. The structure of the n-channel device simulated is illustrated in Fig. 3.1. The uniform body doping density (N_A) was initially set at $2x10^{16}$ cm^{-3}, which is low enough to maintain the fully depleted condition in the subthreshold region for all geometries studied. The front-gate (t_{of}) and back-gate (t_{ob}) oxide thicknesses were 7 nm and 350 nm, respectively. The front gate is n^+ polysilicon, and the back gate is heavily-doped p-type silicon for these simulations. Both SOI film thickness (t_b) and MOSFET channel length (L) are varied independently.

The influence of the short-channel effect on the subthreshold characteristic is assessed first by examining the subthreshold gate swing. In Fig. 3.2 we plot the PISCES-predicted S at low drain bias (V_{DS} = 50 mV) versus L for two values of t_b, showing the loss of the near-ideal slope (S > 60 mV) when the feature size is scaled down to deep-submicron values. For example, for t_b = 100 nm, S increases from 64 mV to 150 mV as L is scaled from 0.7 μm to 0.2 μm. Qualitatively, the nonideal S for short L results partly because increasing the front-gate voltage in the

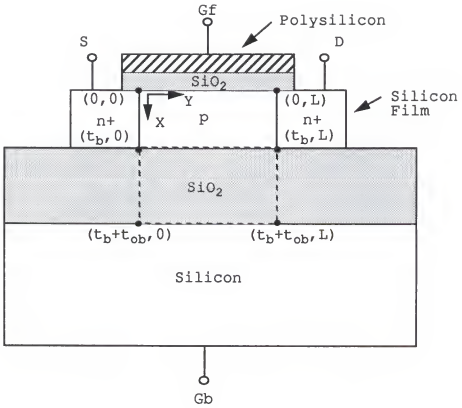


Fig. 3.1 Cross-section of a floating-body n-channel SOI MOSFET

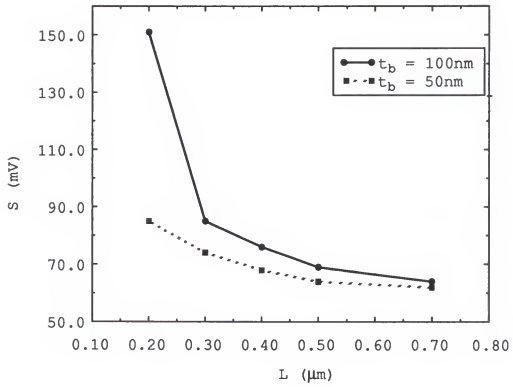


Fig. 3.2 PISCES predicted subthreshold-swing dependences on channel length for different values of film thickness; V_{DS} = 50 mV.

subthreshold region causes more uniform normal field along the front oxide/silicon surface, resulting in less source/drain charge sharing and an increase of effective threshold voltage. For shorter L, S increases more sharply as back-channel current becomes predominant; the threshold voltage of the back surface is more sensitive to the variation of charge sharing than the front surface because of the thicker back oxide. This insight is reflected by the PISCES-simulated equipotential contours and field vectors plotted in Fig. 3.3 for the L = 0.2 μm device biased in the subthreshold region. Note the nonuniform field distribution along the front surface as well as the strongly two-dimensional field in the back oxide. The fringing fields, which are caused by the proximity of the source and drain junctions and influenced by the presence of the (thick) back oxide, tend to induce more inversion charge at the back surface, resulting in significant current flowing through the back channel as shown by the PISCES-predicted current vectors plotted in Fig. 3.4. The increased charge at the back surface will also reduce the front-channel threshold voltage through the charge-coupling effect [Vee88], thus resulting in more leakage current.

It is well known that the short-channel effect in the FD/SOI MOSFET can be effectively reduced by scaling down the film thickness [Vee89]. The S(L) prediction for t_b = 50 nm plotted in Fig. 3.2 illustrates the benefit of scaling t_b for deep-submicron devices; for L = 0.2 μm, S decreases from 150 mV to 86 mV as t_b is thinned from 100 nm. This design flexibility of the FD/SOI MOSFET for controlling the short-

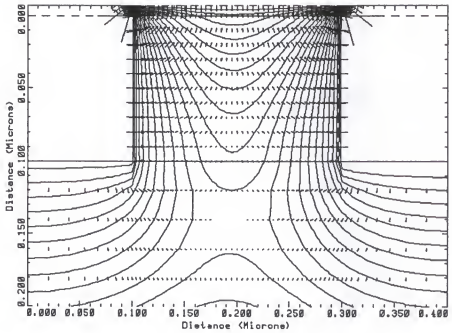


Fig. 3.3 PISCES-simulated equipotential contours and field vectors for a scaled fully depleted n-channel SOI MOSFET biased at V_{GfS} = -0.6V, V_{GbS} = 0, and V_{DS} = 50 mV. L = 0.2 μm, t_b = 100 nm.

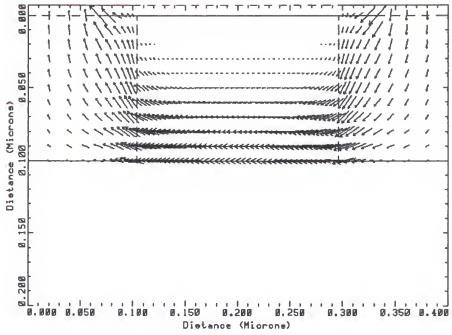


Fig. 3.4 Predicted current vectors from the FD/SOI MOSFET PISCES simulation described in Fig. 3.3.

channel effect is due to the front gate-back gate charge coupling, which tends to constrain the field vertically.

3.3 Subthreshold-Current Model Development

Using the insight from the PISCES study, we now develop a physical subthreshold model for deep-submicron FD/SOI MOSFETs. First, an analytic solution for the potential will be derived based on the two-dimensional analysis in [You89], but extended substantively to account for surface states and other unique mechanisms in fully depleted device as revealed in Section 3.2. For example, we model the effects of fringing fields at the back interface using a DICE-like approach [vee88]. We also model the diffusion of carriers throughout the film body by an innovative charge integration method, accounting for (front and back) channel-length modulation as well. The model is hence capable of predicting the leakage current and subthreshold slope for different channel lengths as well as other structural parameters.

3.3.1 Potential Distribution in the SOI Film

For the n-channel device in Fig. 3.1 operating in the weak-inversion region, Poisson's equation applied to the two-dimensional intrinsic region of the depleted SOI film body ($0 \leq x \leq t_b$, $0 \leq y \leq L$) is

$$\frac{\partial^2}{\partial x^2}\Psi(x,y) + \frac{\partial^2}{\partial y^2}\Psi(x,y) \cong \frac{qN_A}{\varepsilon_s} \quad . \tag{3.1}$$

We stress here that our fully depleted (FD) assumption means not only p, n << N_A as reflected by (3.1), but also that Ψ is not perturbed significantly by a body voltage (V_{BS}) which could result from bias-induced body charging (e.g., via impact ionization [Cho91]). This latter stipulation implies that the body is strongly depleted of holes prior to any charging.

Defining the potential along the front surface [$\Psi(0, y)$] as $\Psi_{sf}(y)$ and the back surface [$\Psi(t_b, y)$] as $\Psi_{sb}(y)$, we use Gauss's law in one dimension to express boundary values for the normal fields as

$$\left.\frac{\partial\Psi}{\partial x}\right|_{x=0} = -E_{sf}(y) = \frac{\varepsilon_{ox}}{\varepsilon_s}\frac{\Psi_{sf}(y)\,(1+qN_{sf}/C_{of}) - (V_{GfS}-V_{FBf})}{t_{of}} \qquad (3.2)$$

and

$$\left.\frac{\partial\Psi}{\partial x}\right|_{x=t_b} = -E_{sb}(y) = \frac{\varepsilon_{ox}}{\varepsilon_s}\frac{(V_{GbS}-V_{FBb}) - \Psi_{sb}(y)\,(1+qN_{sb}/C_{ob})}{t_{ob}} \qquad (3.3)$$

where V_{GfS} and V_{GbS} are the front and back gate-to-source voltages, and V_{FBf} and V_{FBb} are the front- and back-gate flatband voltages, ε_{ox} and ε_s are the dielectric constants of the oxide and silicon, t_{of} and t_{ob} are the front and back gate-oxide thickness, $C_{of} = \varepsilon_{ox}/t_{of}$ and $C_{ob} = \varepsilon_{ox}/t_{ob}$ are the front and back gate-oxide capacitances, and N_{sf} and N_{sb} are the front- and back-gate surface-state densities. The surface states are assumed to be uniformly distributed over the energy gap; that is, the surface charge densities due to the states are $Q_{sf,b} = -qN_{sf,b}\Psi_{sf,b}$. Note that (3.2) and (3.3) implicitly assume vertical fields in the oxides. This

assumption is valid for the front oxide, but not necessarily for the back oxide as evidenced by our PISCES simulations (see Fig. 3.3). Thus an effective $V_{GbS(eff)}$, characterized later by an analysis of the two-dimensional field in the back oxide, will ultimately replace V_{GbS} in (3.3). This extension, essential for deep-submicron devices, further distinguishes this model from that in [You89], which ignores the two-dimensionality of the field in the back oxide.

Following [You89], we assume a second-order parabolic function along the vertical (x) dimension for the solution of (3.1):

$$\Psi(x,y) \equiv \alpha_0(y) + \alpha_1(y)\,x + \alpha_2(y)\,x^2 \tag{3.4}$$

where the coefficients α_i (i = 0, 1, 2) depend on y only. The α_i are expressed, using (3.2) and (3.3), in terms of $\Psi_{sf}(y)$, the mentioned voltages, and the structural capacitances, $C_{of} = \varepsilon_{ox}/t_{of}$, $C_{ob} = \varepsilon_{ox}/t_{ob}$, and $C_b = \varepsilon_s/t_b$. Then substituting (3.4) into (3.1) yields a second-order differential equation in x in terms of $\Psi_{sf}(y)$. The appropriate boundary conditions are defined at the metallurgical source (y = 0) and drain (y = L) junctions:

$$\Psi_{sf}(0) = \Psi_b \tag{3.5}$$

and

$$\Psi_{sf}(L) = \Psi_b + V_{DS} \tag{3.6}$$

where $\Psi_b = V_t \ln(N_A N_{SD}/n_i^2)$ is the built-in potential of the source/drain-body junctions; N_{SD} is the source/drain (or LDS/LDD) doping density and $V_t = kT/q$ is the thermal voltage. Note in (3.5) and (3.6) that we have neglected any V_{BS} since, for our strongly FD assumption, its effect on channel conduction is negligible. Of course for V_{DS} high enough, V_{BS} will drive the parasitic BJT-induced breakdown or latch of the device [Cho91].

With (3.5) and (3.6), the derived differential equation is solved for $\Psi_{sf}(y)$, which is then substituted into the α_i expressions in (3.4), yielding a solution for the potential of the form

$$\Psi(x,y) = \frac{\left[1-e^{-(2A'')^{0.5}L}\right](K''+\Psi_b)+V_{DS}}{2\sinh\left[(2A'')^{0.5}L\right]} e^{(2A'')^{0.5}y} + \frac{\left[e^{(2A'')^{0.5}L}-1\right](K''+\Psi_b)-V_{DS}}{2\sinh\left[(2A'')^{0.5}L\right]} e^{-(2A'')^{0.5}y} - K'' \qquad (3.7)$$

where

$$A''(x) = \frac{1}{A^{-1}\left(1+\frac{C_{of}r_f}{\varepsilon_s}x\right)-x^2} \qquad (3.8)$$

$$K''(x) = \left[C''(V_{FBb}-V_{GbS})-B''(V_{GfS}-V_{FBf})+\frac{qN_A}{2\varepsilon_s}\right]/A'' \qquad (3.9)$$

$$B''(x) = A''\left(-\frac{C_{of}}{\varepsilon_s}x+Bx^2\right)+B \qquad (3.10)$$

and

$$C''(x) = C\left(1 + A''x^2\right) \quad . \tag{3.11}$$

A, B, and C in (3.8) - (3.11) are constants dependent on C_{of}, C_{ob}, and C_b, as well as N_{sf} and N_{sb}:

$$A = \frac{r_b + \frac{C_{of}}{C_{ob}} r_f + \frac{C_{of}}{C_b} r_f r_b}{t_b^2\left(r_b + 2\frac{C_b}{C_{ob}}\right)}, \tag{3.12}$$

$$B = \frac{\frac{C_{of}}{C_{ob}} + \frac{C_{of}}{C_b} r_b}{t_b^2\left(r_b + 2\frac{C_b}{C_{ob}}\right)}, \tag{3.13}$$

and

$$C = \frac{1}{t_b^2\left(r_b + 2\frac{C_b}{C_{ob}}\right)} \tag{3.14}$$

where $r_f = 1 + qN_{sf}/C_{of}$ and $r_b = 1 + qN_{sb}/C_{ob}$. The solution $\Psi(x,y)$ in (3.7) is what we need to model the subthreshold current in the FD device. Note for L very long and/or t_b very thin, $\Psi \cong -K''$ over most of the channel length; this simpler result is the solution of Poisson's equation in one (vertical) dimension [Vee88]. Thus our general solution (3.7) is scalable with the device structure.

3.3.2 Fringe-Field Analysis in the Underlying Oxide

To complete the characterization of $\Psi(x,y)$ though, we need to define $V_{GbS(eff)}$ to replace V_{GbS} in (3.3) by accounting for the two-dimensionality of the electric field in the back underlying oxide, which tends to support the back-surface inversion. With reference to Fig. 3.1, Laplace's equation applied to the oxide, with negligible charge, is

$$\frac{\partial^2}{\partial x^2}\Psi(x,y) + \frac{\partial^2}{\partial y^2}\Psi(x,y) \cong 0 \tag{3.15}$$

for $t_b \leq x \leq t_b+t_{ob}$ and $0 \leq y \leq L$. The boundary conditions are $\Psi(t_b,y) = \Psi_{sb}(y)$, $\Psi(t_b,0) = \Psi_b$, and $\Psi(t_b,L) = \Psi_b + V_{DS}$; the boundary condition at the back oxide/substrate interface $[\Psi(t_b+t_{ob},y)]$ can be derived by writing the potential balance equation between the substrate and source regions:

$$V_{GbS} = -\Phi_{Msub} + \Psi_{ob}(y) + \Psi_{sb}(y) + \Psi_b \tag{3.16}$$

where Φ_{Msub} is the work-function difference between the source region and substrate, and Ψ_{ob} is the potential drop across the back oxide. Therefore, we have

$$\Psi(t_b+t_{ob},y) \equiv \Psi_{ob}(y) + \Psi_{sb}(y) = V_{GbS} - \Phi_{MSb} \tag{3.17}$$

where Φ_{MSb} $(= -\Phi_{Msub} + \Psi_b)$ is the work-function difference between the substrate and the film body. The above condition ignores the possibility of charge induced in the (high-resistivity) silicon substrate. However, because t_{ob} is relatively thick, the associated surface potential in the

substrate will typically not exceed the (small) Fermi potential, and hence will not significantly affect the solution to (3.1).

To derive an analytic estimate for the solution to (3.15), we use a quasi-two-dimensional analysis like that for DICE in [Vee88]; we assume that the two partial derivatives are not strongly coupled:

$$\frac{\partial^2}{\partial x^2}\Psi(x,y) \cong -\frac{\partial^2}{\partial y^2}\Psi(x,y) \cong -\eta \tag{3.18}$$

where η is an empirical constant that must approach zero as L increases. Integrating (3.18) from y = 0 to y = L yields

$$\begin{aligned}\eta &= \frac{2}{L^2}\left[\Psi(x,L) - \Psi(x,0) - \left.\frac{\partial\Psi(x,y)}{\partial y}\right|_{y=0} L\right] \\ &\cong \frac{2}{L^2}(\kappa V_{DS} + \gamma E_0 L)\end{aligned} \tag{3.19}$$

where $E_0 (\equiv -\partial\Psi/\partial y|_{x=t_b,\, y=0})$ represents the source of the fringing field; γ and κ are constant weighting factors used to define effective lateral boundary conditions independent of x in the oxide. Both of the weighting factors should be ≤ 1 in accord with the boundary conditions at $x = t_b$ and $x = t_b + t_{ob}$.

Next we integrate (3.18) from $x = t_b$ to $x = t_b + t_{ob}$, getting the vertical field $E_s(y)$ $(= -\partial\Psi/\partial x|_{x=t_b})$ at the SOI interface:

$$E_s(y) = \frac{1}{t_{ob}}\left[\Psi_{sb}(y) - V_{GbS} + \Phi_{MSb} - \frac{t_{ob}^2}{L^2}(\kappa V_{DS} + \gamma E_0 L)\right]. \tag{3.20}$$

We note here that the values of γ and κ, which depend only on t_{ob}, can be determined from numerical device simulations at low V_{DS} for γ and at $V_{DS} = V_{DD}$ for κ. Table 3.1 presents the extracted values of γ and κ versus back-oxide thickness based on the PISCES-predicted subthreshold characteristics. (For t_{ob} not listed in table, the values of γ and κ can be linearly interpolated between given values.) With (3.20), we relate E_s to the back surface field E_{sb} in the silicon film via Gauss's law, and generalize the boundary condition in (3.3) to account for the two-dimensional field in the back oxide:

$$\left.\frac{\partial \Psi}{\partial x}\right|_{x = t_b} = \frac{\varepsilon_{ox}}{\varepsilon_s} \frac{(V_{GbS(eff)} - V_{FBb}) - r_b \Psi_{sb}(y)}{t_{ob}} \tag{3.21}$$

with

$$V_{GbS(eff)} \equiv V_{GbS} + \frac{t_{ob}^2}{L^2}(\kappa V_{DS} + \gamma E_0 L) \tag{3.22}$$

for the effective back-gate bias, which will reduce to V_{GbS} for long L and/or thin t_{ob}. Note now that since the final solution in (3.7) depends on $V_{GbS(eff)}$, which in (3.22) depends on $\Psi(x,y)$ via E_0, a numerical iterative loop is required to derive the potential. However we have found a good tradeoff between accuracy and computation time is effected by using only one iteration since E_0 is only slightly sensitive to V_{GbS}.

Table 3.1
PISCES-Extracted Weighting Factors

standard t_{ob} (nm)	γ	κ
350	0.3	0.5
200	0.5	0.7
100	0.7	0.9
≤50	1.0	1.0

3.3.3 Current Derivation

The derived potential distribution is now used to model the subthreshold current. For weak inversion, we model the diffusion current along an effective channel length ($L_e < L$); its density (J_n) is approximately [Sze81]

$$J_n \cong qD_n \frac{n(L_s)}{L_e}\left(1 - e^{-V_{DS}/V_t}\right) \tag{3.23}$$

where $n(L_s)$ is the electron density at the virtual source where $\Psi(y)$ is minimum. The effective channel length is defined as $L_e \equiv L - L_s - L_d + 2L_D$, where L_s and L_d reflect the encroachments of the depletion regions associated with the source and drain junctions, and L_D is a Debye length. The encroachments are estimated using our solution for $\Psi(x,y)$ as follows:

$$L_s \cong \frac{2\left[\Psi_b - \Psi_{s(min)}\right]}{\left|\frac{\partial \Psi(x,y)}{\partial y}\right|_{y=0}} \tag{3.24}$$

and

$$L_d \cong \frac{2\left[\Psi_b - \Psi_{s(min)} + V_{DS}\right]}{\left|\frac{\partial \Psi(x,y)}{\partial y}\right|_{y=L}} \tag{3.25}$$

where $\Psi_{s(min)}$ is the minimum surface potential at $y = y_m$ between the source and drain. Including the Debye length L_D (defined by N_A) in the definition of L_e accounts for the transition regions separating drift and diffusion regions of the channel [Tay78], as well as defining a physical limitation on L_e when $(L_s + L_d) \rightarrow L$.

The total weak-inversion current I_{WK} is obtained by integrating (3.23) over the entire SOI film thickness, and is partitioned into front- and back-surface components (I_{WKf} and I_{WKb}) to simplify the formalism:

$$I_{WK} = W\int_0^{t_b} J_n dx$$

$$\cong I_{WKf}(0 \le x \le x_{min}) + I_{WKb}\left(x_{min} \le x \le t_b\right)$$

$$\cong WV_t\left(\frac{\overline{\mu_{nf}}Q_{nf}\Big|_{y=L_{sf}}}{L_{ef}} + \frac{\overline{\mu_{nb}}Q_{nb}\Big|_{y=L_{sb}}}{L_{eb}}\right)\left(1-e^{-V_{DS}/V_t}\right) \qquad (3.26)$$

where x_{min} is the partition point, which is defined by the smaller of minimum potentials of $\Psi(x,y_{mf})$ and $\Psi(x,y_{mb})$ between x = 0 to x = t_b, and has implicitly included process/bias dependence. Q_{nf} and Q_{nb} are the partitioned channel charges, which are estimated adequately at the virtual sources (L_{sf} and L_{sb}) by assuming linear variations of potential in x between the (front and back) surfaces and x_{min} as illustrated in Fig. 3.5; $\overline{\mu_{nf}}$ and $\overline{\mu_{nb}}$ are average electron mobilities [Vee88]. The electron density, $n \cong (n_i^2/N_A)\exp(\Psi/V_t)$, is defined by $\Psi(x,y)$; hence [for x_{min} defined by $\Psi(x, y_{mf})$ as in Fig. 3.5],

$$Q_{nf}\Big|_{y=L_{sf}} \cong q\int_0^{x_{min}} n(x,y_{mf})\,dx$$

$$= q\int_{\Psi_{sf(min)}}^{\Psi\left(x_{min},y_{mf}\right)} n(x,y_{mf})\,d\Psi\frac{dx}{d\Psi}\Big|_{y=y_{mf}}$$

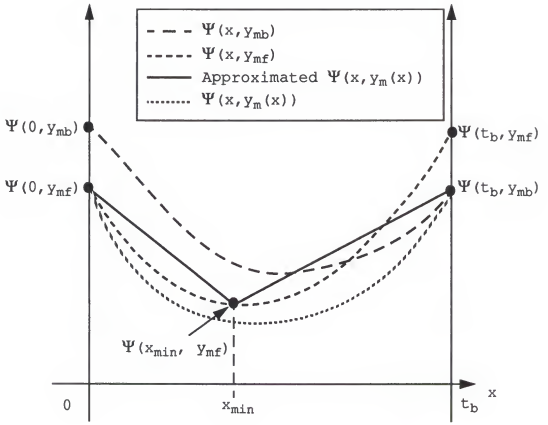


Fig. 3.5 Representative potential variations (in x at y_{mf} and y_{mb}) in the FD/SOI film body, and corresponding linear approximations; $\Psi(x, y_m(x))$ represents the diffusion-source potential at arbitrary x.

$$\cong \frac{q\left(\frac{n_i^2}{N_A}\right)V_t x_{min}}{\Psi_{sf(min)} - \Psi(x_{min}, y_{mf})}\left\{\exp\left[\frac{\Psi_{sf(min)}}{V_t}\right] - \exp\left[\frac{\Psi(x_{min}, y_{mf})}{V_t}\right]\right\}, \tag{3.27}$$

which is approximated using $n(x, y_{mf})$ to maintain consistency with the long-channel device. Also [for x_{min} defined by $\Psi(x, y_{mf})$ as in Fig. 3.5],

$$Q_{nb}\Big|_{y=L_{sb}} \cong q\int_{x_{min}}^{t_b} n(x, y_{mb})\,dx$$

$$\cong \frac{qn_i^2 V_t}{N_A}\frac{\sqrt{(t_b - x_{min})^2 + (y_{mf} - y_{mb})^2}}{\Psi_{sb(min)} - \Psi(x_{min}, y_{mf})}$$

$$\cdot\left\{\exp\left[\frac{\Psi_{sb(min)}}{V_t}\right] - \exp\left[\frac{\Psi(x_{min}, y_{mf})}{V_t}\right]\right\}. \tag{3.28}$$

Note that the integration in (3.28) is done quasi-two-dimensionally, that is, from (x_{min}, y_{mf}) to (t_b, y_{mb}), by modifying $d\Psi/dx|_{y=ymb}$ based on the Pythagorean theorem. Although this modification tends to misrepresent the exact diffusion-source potential $\Psi[x, y_m(x)]$ (see Fig. 3.5) at arbitrary x, the related error in charge calculation is insignificant because of the predominant exponential dependences on surface potential in (3.27) and (3.28) involving the properly defined partitioned point.

3.4 Modifications of Strong-Inversion Analysis for Including Surface States

Previous strong-inversion modeling does not account for the surface-state charge densities at the front and back surfaces [Vee88]. To be consistent with our subthreshold modeling and to render the model applicable to actual technology, it is in order to revise the strong-inversion analysis by including the surface-state charges. The approach is straightforward; it is to add the surface-state charges Q_{sf} and Q_{sb} (as defined in Section 3.3) to the original one-dimensional boundary conditions defined by Gauss's law as follows:

$$\varepsilon_S E_{sf} - \varepsilon_{OX} E_{of} = Q_{nf} + Q_{of} + Q_{sf} \tag{3.29}$$

and

$$\varepsilon_S E_{sb} - \varepsilon_{OX} E_{ob} = Q_{ob} + Q_{sb} \tag{3.30}$$

where E_{of} and E_{ob} are the normal fields in the front and back oxides, Q_{nf} is the front-channel inversion-layer charge per unit area, and Q_{of} and Q_{ob} are the front and back fixed oxide charges per unit area. Following [Vee88], we neglect the back-channel charge and write

$$Q_{nf} = -C_{of}\left[V_{GfS} - V_{FBf} - \left(r_f + \frac{C_b}{C_{of}}\right)\Psi_{sf} + \frac{C_b}{C_{of}}\Psi_{sb} + \frac{Q_{b(eff)}}{2C_{of}}\right] \tag{3.31}$$

and

$$0 = -C_{ob}\left[V_{GbS} - V_{FBb} + \frac{C_b}{C_{ob}}\Psi_{sf} - \left(r_b + \frac{C_b}{C_{ob}}\right)\Psi_{sb} + \frac{Q_{b(eff)}}{2C_{ob}}\right] \tag{3.32}$$

for $V_{DS} = 0$; $Q_{b(eff)}$ is the effective charge per unit area defined by the front gate [Vee88]. Substituting (3.32) into (3.31) yields

$$Q_{nf} = -C_{of}\left[V_{GfS} - V_{FBf} - r_f(1+\alpha)\Psi_{sf} + \frac{\alpha}{r_b}(V_{GbS} - V_{FBb}) + \frac{\beta Q_{b(eff)}}{2C_{of}}\right] \quad ; \tag{3.33}$$

$\alpha = C_b r_b C_{ob}/(r_f C_{of}(C_b + r_b C_{ob}))$ and $\beta = 1 + C_b/(C_b + r_b C_{ob}) r_f$ are charge-coupling factors. (Note that for negligible N_{sf} and N_{sb}, i.e., $r_f = r_b = 1$, α and β become the previously defined coupling factors in [Vee88].) When compared to the ideal case of no surface-state charges, Eq. (3.33) reveals that the front (n-) channel is less inverted since the same gate voltage (V_{GfS}) has to support the additional surface-state charges. The charge-coupling expression (3.33), as well as boundary equations (3.29) and (3.30), are the key equations for modifying the strong-inversion formalisms discussed in [Vee88]. For example, following the same physical analysis in [Vee88], we now write the expression for the channel charge (ΔQ_{nf}) modulated by DICE, in terms of modulated surface potential $\Delta\Psi_{sf}$, as

$$\Delta Q_{nf} = C_{of} r_f (1+\alpha)\Delta\Psi_{sf} - \beta\frac{\epsilon_s r_b V_{DS}}{L^2} \quad , \tag{3.34}$$

which will converge to the previous result in [Vee88] if both N_{sf} and N_{sb} are negligible.

3.5 Moderate-Inversion Analysis

To complete the subthreshold conduction model, we account for moderate inversion via a cubic polynomial interpolation [Cha87], which links the weak-inversion current to our previously developed strong-inversion current [Vee88] to ensure continuous channel current and transconductance. The boundaries of the moderate-inversion region are physically defined and varied by terminal bias; they determine the width of the transition region, which tends to be a large fraction of supply voltage in deep-submicron circuits, and hence becomes important for precise prediction of performance.

3.5.1 Boundaries of the Moderate-Inversion Region

The boundaries of the moderate-inversion (transition) region are values of V_{GfS} that correspond to the physical onsets of weak and strong inversion. According to the analysis of this region in [Tsi82], the potential boundary between weak and moderate inversion is close to $2\Phi_B$, where Φ_B is the Fermi potential defined by N_A. Our insight gained from the PISCES simulations suggests that this boundary (Ψ_{sfW} for front surface and Ψ_{sbW} for back surface) be defined as $\Psi_{sf,bW} = 2\Phi_B - mV_t$ with $m \cong 5$. Then we obtain the value of V_{GfS} corresponding to $\Psi_{sf(min)} = \Psi_{sfW}$, defined as V_{TWf}, directly (but via numerical iteration) from the solution $\Psi(x,y)$ in (3.7), which includes V_{DS} dependence. Analogously, we obtain V_{TWb}, which is the value of V_{GfS} corresponding to $\Psi_{sb(min)} =$

Ψ_{sbW}. The effective boundary-voltage (V_{TW}) between weak and moderate inversion then is defined as the minimum value of V_{TWf} and V_{TWb}.

To define the boundary between moderate and strong inversion, we write, from (3.33)

$$V_{GfS} = V_{FBf} - (V_{GbS} - V_{FBb})\frac{\alpha}{r_b} + \Psi_{sf}(r_f + \alpha) + \frac{\beta q N_{A(eff)} t_b - 2Q_{nf}}{2C_{of}} \quad (3.35)$$

for $V_{DS} = 0$, where $N_{A(eff)}$ defines the body depletion charge effectively supported by the front gate, which is characterized by an empirical source/drain charge-sharing model [Vee88]. To find the inversion-layer charge per unit area, Q_{nf}, we apply the one-dimensional Poisson's equation in the SOI film region:

$$\frac{\partial^2 \Psi}{\partial x^2} \cong \frac{qN_A}{\varepsilon_s}\left[\exp\left(\frac{\Psi - 2\Phi_B}{V_t}\right) + 1\right] , \quad (3.36)$$

which includes inverted electrons and ionized acceptors in the (depleted) body. Multiplying both sides of (3.36) by $2(d\Psi/dx)$ and integrating over the thin film yields

$$E_{sf}^2 - E_{sb}^2 = \frac{2qN_A V_t}{\varepsilon_s}\left\{\exp\left(\frac{-2\Phi_B}{V_t}\right)\left[\exp\left(\frac{\Psi_{sf}}{V_t}\right) - \exp\left(\frac{\Psi_{sb}}{V_t}\right)\right] + \frac{\Psi_{sf} - \Psi_{sb}}{V_t}\right\} \quad (3.37)$$

with $E_{sf,b}$ representing the transverse electric field at the surface. In strong inversion we can assume $E_{sb} << E_{sf}$ and $\Psi_{sb} << \Psi_{sf}$ because of the thick back oxide; the front-surface field then can be estimated from (3.37):

$$E_{sf} \cong \sqrt{\frac{2qN_A V_t}{\varepsilon_s}\left[\frac{\Psi_{sf}}{V_t} + \exp\left(\frac{\Psi_{sf}-2\Phi_B}{V_t}\right)\right]} \quad . \tag{3.38}$$

Applying Gauss's law in one dimension to the thin film then gives

$$Q_{nf} \cong -Q_r\sqrt{\frac{\Psi_{sf}}{V_t} + \exp\left(\frac{\Psi_{sf}-2\Phi_B}{V_t}\right)} + qN_A t_b \tag{3.39}$$

where $Q_r = \sqrt{2q\varepsilon_s N_A V_t}$.

Next we need to define the potential boundary between moderate and strong inversion. Differentiating (3.35) with respect to V_{GfS}, we have

$$\frac{d\Psi_{sf}}{dV_{Gfs}} = \frac{C_{of}}{(r_f+\alpha)C_{of}+C_{if}} \tag{3.40}$$

where $C_{if} = -dQ_{nf}/d\Psi_{sf}$. As noted in [Tsi82], at the boundary between moderate and strong inversion the slope of Q_{nf} vs. V_{GfS} approaches the constant value equal to $-C_{of}$; that is

$$\frac{dQ_{nf}}{dV_{Gfs}} = \frac{-C_{of}C_{if}}{(r_f+\alpha)C_{of}+C_{if}} \cong -C_{of}\,. \tag{3.41}$$

We then define the strong-inversion lower limit as the value of potential (Ψ_{sfS}) where $C_{if} = 10(r_f+\alpha)C_{of}$, implying the slope at this boundary is 0.91 times $-C_{of}$. With (3.39), this criterion yields

$$\frac{Q_r\left[1+\exp\left(\frac{\Psi_{sfS}-2\Phi_B}{V_t}\right)\right]}{2V_t\sqrt{\frac{\Psi_{sfS}}{V_t}+\exp\left(\frac{\Psi_{sfS}-2\Phi_B}{V_t}\right)}} - 10(r_f+\alpha)C_{of} = 0\,, \tag{3.42}$$

where the value of Ψ_{sfS} can be obtained from approximately four straight (fixed-point) iterations.

The value of V_{Gfs} (defined as V_{TS0}) corresponding to Ψ_{sfS} can now be extracted from (3.35) by replacing Ψ_{sf} with Ψ_{sfS} and using (3.39). Application of a drain bias will alter this boundary since Q_{nf} will be modulated by DICE [Vee88]. The implied reduction of V_{TS0} is proportional to the increase of Q_{nf} at the source [Vee89]; that is,

$$V_{TS} = V_{Ts0} - \frac{\beta \varepsilon_s t_b V_{DS}}{C_{of} L^2} \quad . \tag{3.43}$$

3.5.2 Channel Current

Based on the defined physical boundaries of the moderate-inversion region, the log of the channel current (I_{CH}) is now interpolated via a third-order polynomial [Cha87] between V_{TW} and V_{TS}:

$$\ln(I_{CH}) = \beta_0 + \beta_1 (V_{Gfs} - V_{TW}) + \beta_2 (V_{Gfs} - V_{TW})^2 + \beta_3 (V_{Gfs} - V_{TW})^3 \tag{3.44}$$

where the coefficients β_i (i = 0,1,2,3) are evaluated to ensure continuous current and its derivative (with respect to V_{Gfs}) at the boundaries; thus

$$\beta_0 = \ln[I_{CH}^{WK}(V_{TW})] , \tag{3.45}$$

$$\beta_1 = \frac{d \ln[I_{CH}^{WK}(V_{TW})]}{dV_{Gfs}} , \tag{3.46}$$

$$\beta_2 = 3\frac{\ln\left[\frac{I_{CH}^{ST}(V_{TS})}{I_{CH}^{WK}(V_{TW})}\right]}{(V_{TS}-V_{TW})^2} - \left\{\frac{\frac{d\ln[I_{CH}^{ST}(V_{TS})]}{dV_{Gfs}} + 2\frac{d\ln\left[I_{CH}^{WK}(V_{TW})\right]}{dV_{Gfs}}}{V_{TS}-V_{TW}}\right\}, \qquad (3.47)$$

and

$$\beta_3 = 2\frac{\ln\left[\frac{I_{CH}^{WK}(V_{TW})}{I_{CH}^{TS}(V_{TS})}\right]}{(V_{TS}-V_{TW})^3} - \left\{\frac{\frac{d\ln\left[I_{CH}^{ST}(V_{TS})\right]}{dV_{Gfs}} + \frac{d\ln\left[I_{CH}^{WK}(V_{TW})\right]}{dV_{Gfs}}}{(V_{TS}-V_{TW})^2}\right\}. \qquad (3.48)$$

Both derivatives in weak and strong inversion are calculated numerically, as discussed in Chapter 4.

3.6 Charge Modeling

The FD/SOI MOSFET model is charge-based, relying on the quasi-static approximation which assumes the variation of terminal voltage is slow enough for the charge to retain its DC voltage dependences. The charging/discharging current at each terminal then can be expressed as

$$\frac{dQ_i}{dt} = \sum_j \frac{\partial Q_i}{\partial V_j}\frac{dV_j}{dt} \qquad (3.49)$$

where i = Gf, Gb, S or D and j= GfS, GbS and DS; in accord with the FD assumption, the body charge is assumed fixed. The weak-inversion charges are evaluated based on our potential solution $\Psi(x,y)$ and charge neutrality, and linked to the strong-inversion charge model [Vee88] via linear interpolation to account for the moderate-inversion charge.

The model also physically includes bias-dependent substrate depletion charge under the source and drain regions to characterize the effective source/drain capacitances for scaled-box devices.

3.6.1 Intrinsic Weak-Inversion Terminal Charges

The voltage dependences of the integrated charges (neglecting extrinsic components) associated with the five terminals, Q_{Gf}, Q_{Gb}, Q_S, Q_D and Q_B, in the weak-inversion region are evaluated based on our potential solution $\Psi(x,y)$ and neutrality. The front-gate charge (Q_{Gf}) is obtained by applying Gauss's law and integrating along the front channel:

$$Q_{Gf} = WC_{of}\int_0^L [V_{GfS} - \Phi_{MSf} - \Psi_{sf}(y)]\,dy \qquad (3.50)$$

where Φ_{MSf} is the work-function difference between the front gate and film body. For V_{GfS} well below threshold, the film body might be partially depleted or even accumulated, which is inconsistent with (3.1) and our solution for $\Psi(x,y)$. In order to maintain charge continuity, we define an effective onset of accumulation as the value of V_{GfS} at which Q_{Gf} in (3.50) equals $WLC_{of}(V_{GfS} - \Phi_{MSf})$, and use this expression for Q_{Gf} for all V_{GfS} below this onset. Physically the accumulation charge should be reflected by the body charge (Q_B) as well as Q_{Gf}. However this perturbation of Q_B, which would have to be supported by (slow) carrier generation in the floating-body device, is neglected, and the excess

charge in Q_{Gf} is assumed to be imaged in Q_{Gb}. Hence, consistent with the model assumptions, we assume fixed $Q_B = -WLqN_At_b$. (The charge associated with the parasitic BJT [Cho91] is assumed to be relatively insignificant.) Also for weak inversion, the channel charge is negligible and hence so are the intrinsic source and drain charges ($Q_S \cong Q_D \cong 0$). Thus Q_{Gb} can be determined from the charge-neutral condition:

$$Q_{Gf} + Q_{Gb} + Q_B + Q_{ff} + Q_{fb} \cong 0 \tag{3.51}$$

where Q_{ff} and Q_{fb} are the fixed front- and back-oxide charges.

In (3.51) we have neglected the surface-state charge at the front oxide/silicon interface because the surface-state density associated with thermally grown (front) oxide is always small. We also argue that the back surface-state charge can be ignored for the following reason. Physically, the back surface-state charge (Q_{sb}) is supported (partitioned) by the charges injected from the source (Q_{sbS}), drain (Q_{sbD}), and body (Q_{sbB}) regions. In weak inversion, we differentiate (3.51) with time and obtain

$$\frac{dQ_{Gf}}{dt} + \frac{dQ_{Gb}}{dt} + \frac{dQ_{sbS}}{dt} + \frac{dQ_{sbD}}{dt} = 0 \tag{3.52}$$

by adding the surface-state charging currents. (Note that the body charge is assumed fixed.) Regarding the charging components supported by the source (dQ_{sbS}/dt) and drain (dQ_{sbD}/dt), since the values of those charges are linearly dependent on the back-surface potential, their transient

rates of change should be less than those of the partitioned channel charges (Q_S and Q_D), which have exponential dependences on potential and are ignored. Furthermore, the displacement current associated with the front gate (dQ_{Gf}/dt), which implicitly accounts for the surface states through Ψ_{sf} in (3.50), will dominate the charging currents because of large front-oxide capacitance. Given this insight, (3.52) can be simplified to

$$\frac{dQ_{Gf}}{dt} + \frac{dQ_{Gb}}{dt} \equiv 0 \quad . \tag{3.53}$$

Note that (3.53) implies that the positive charges induced on the front gate due to Q_{sb} now has to be neutralized by the electrons flowing into the back gate. Although this is non-physical charge dynamics for the back gate, the effect is minimized in circuit operation because dQ_{Gb}/dt usually is not significant in circuit operation.

In strong inversion, the charging currents due to back surface states are overwhelmed by the transient channel currents dQ_S/dt and dQ_D/dt. All this then suggests that no modification to the previous charge expressions is required due to the surface states; hence the simplicity and efficiency of the charge model is retained.

3.6.2 Intrinsic Moderate-Inversion Terminal Charges

The terminal charges associated with the moderate-inversion region are approximated by using linear-interpolation between the boundaries V_{TW} and V_{TS}:

$$Q_X = Q_{XW} + (V_{GfS} - V_{TW})\frac{Q_{XS} - Q_{XW}}{V_{TS} - V_{TW}} \tag{3.54}$$

where X = Gf, Gb, S or D. Q_{XS} and Q_{XW} are the strong- and weak-inversion boundary charges. The linear relationship of Q_X with V_{GfS} implies that the derivative of charge, or related capacitance, will be constant in the transition region, which is non-physical, yet adequate in digital applications as long as the supply voltage is larger than V_{TS}. It implies that the integrated charge in the transition region equals $Q_{XS} - Q_{XW}$.

3.6.3 Source/Drain Substrate Depletion Charges

Gate overlap capacitances define extrinsic components of Q_S and Q_D as well as Q_{Gf} and Q_{Gb}, which have been modeled in [Vee88] by simple oxide capacitances. However, consider $Q_{S(Gb)}$ and $Q_{D(Gb)}$ due to the back gate (substrate), which characterize the MOS capacitance under the source and drain regions. Since the substrate is generally lightly doped (p-type) in SOI technology, the characterization must account for possible charge in the substrate. Applying Gauss's law to the underlying MOS structure yields

$$Q_{S(Gb)} = C_{ob}\left(-V_{GbS} - \Phi_{Msub} - \Psi^S_{sub}\right)A_S \tag{3.55}$$

$$Q_{D(Gb)} = C_{ob}\left(V_{DS} - V_{GbS} - \Phi_{Msub} - \Psi^D_{sub}\right)A_D \tag{3.56}$$

where Φ_{Msub} is the work-function difference between the source/drain region and the substrate, $\Psi_{sub}^{S,D}$ is the surface band bending relative to the substrate at the oxide/silicon interface under the source/drain region, and $A_{S,D}$ is the effective area of the source/drain region. The depletion approximation [Sze81] is used to model $\Psi_{sub}^{S,D}$ and thus $Q_{S(Gb)}$ and $Q_{D(Gb)}$. The condition of accumulation in the substrate is accounted for by assuming $\Psi_{sub}^{S,D} = 0$ in (3.55) and (3.56), but inversion charge is neglected since there is no source of minority carriers, and deep depletion, which is accounted for, is more likely.

The charge model is hence supplemented based on (3.55) and (3.56): $Q_S = Q_S + Q_{S(Gb)}$ and $Q_D = Q_D + Q_{D(Gb)}$; and $Q_{Gb} = Q_{Gb} - Q_{S(Gb)} - Q_{D(Gb)}$ in accord with neutrality. Note that this extrinsic charge modeling reflects how the source/drain capacitance of the thin-film SOI MOSFET is equivalently a series combination of the back-oxide capacitance ($C_{ob} = \varepsilon_{ox}/t_{ob}$) and the substrate depletion capacitance [All93]. Since the substrate is lightly doped in common SOI technology, the source/drain capacitance is hence not strongly sensitive to t_{ob} and will always be less than that of bulk-silicon MOSFETs, irrespective of t_{ob}.

3.7 Summary

Based on numerical device simulations and provided physical insight, we developed a new subthreshold model for the FD/SOI MOSFET. In order to model the weak-inversion current properly for circuit simulation, we derived a two-

dimensional analytic solution for the potential, physically accounting for source/drain charge sharing and including the effects on the back SOI surface boundary condition of fringing fields from the source and drain junctions in the underlying (back) oxide. We accounted for the diffusion of carriers throughout the thin-film body, including back-surface current which underlies any substantive deterioration of the subthreshold slope and leakage current. The new current model was supplemented with the related charge modeling. Substrate charge (under source/drain regions) was included based on the depletion approximation. The weak-inversion model is interpolated across the moderate-inversion region, linking it to our previously developed strong-inversion formalism [Vee88]. The models are implemented in SOI-SPICE, as well as verified by two-dimensional numerical device simulation and experiment in the following chapter.

CHAPTER 4
MODEL IMPLEMENTATION/VERIFICATION

4.1 Introduction

This chapter describes the implementation of our developed subthreshold current/charge model into the SOISPICE-2 circuit simulator, which creates "SOI-SPICE-4" (Ver. 4.1) [Fos95]. The program has also been extended by adding a partially depleted (PD) SOI MOSFET model [Suh95], enabling both FD and PD device/circuit simulation.

The new subthreshold fringing-field analysis and moderate-inversion calculation are more intensive than that in SOISPICE-2, and therefore are implemented as an option which is turned on and off by user-specified model parameters. In Section 4.2 we give detailed descriptions on the implemented model algorithm, and list source-code modifications in the original SOISPICE subroutines as well. Comparison between model and two-dimensional numerical simulations of scaled devices with varying structural dimensions are presented in Section 4.3, verifying the capability of SOI-SPICE-4 in predicting deep-submicron FD/SOI device performance. Finally, a simple algorithm for parameter evaluation is described in Section 4.4 to facilitate measurement verifications and model utility.

4.2 Model Implementation in SOI-SPICE-4

4.2.1 Model Algorithm

Fig. 4.1 shows the overall algorithm of new model routine SOIMOD. In general, SOIMOD is similar to the previous model routine (retained and now called SOIMOD_3) in the strong-inversion analysis [Cho91], but upgraded by including the moderate-inversion and two-dimensional weak-inversion analyses. A Newton-like loop is included to account for the non-ohmic voltage drop analysis in the LDD region [Cho91], while the ohmic resistances associated with LDD and LDS are added directly to the admittance matrix (in SOIFET) to simplify the iterative analysis in the model routine and to improve convergence speed.

From the beginning, the terminal voltage differences V_{GfS}, V_{GbS}, V_{DS} and V_{BS}, derived from the SPICE nodal analysis are passed into the model routine after each Newton-Raphson iteration. The strong-inversion boundary V_{TS} is then found from (3.43) by replacing Ψ_{sf} with Ψ_{sfS} defined in (3.42). If the device is biased below the strong-inversion boundary, the weak-inversion boundary V_{TW} is calculated, based on Ψ_{sW}, via numerical iteration due to the nonlinear relation between $\Psi_{s(min)}$ and V_{GfS} in (3.7), which includes the implicit fringing-field dependence of $V_{GbS(eff)}$ ((3.22)). A straight iteration on position y_m (corresponding to $\Psi_{s(min)}$), which we found to be more efficient than solving V_{TW} from (3.7) via the secant method, is used. It is performed by first assuming an initial guess of y_m (= 0.5L), then extracting V_{TW} from (3.7) with $\Psi_{s(min)} = \Psi_{sW}$. The value of V_{TW} is then substituted

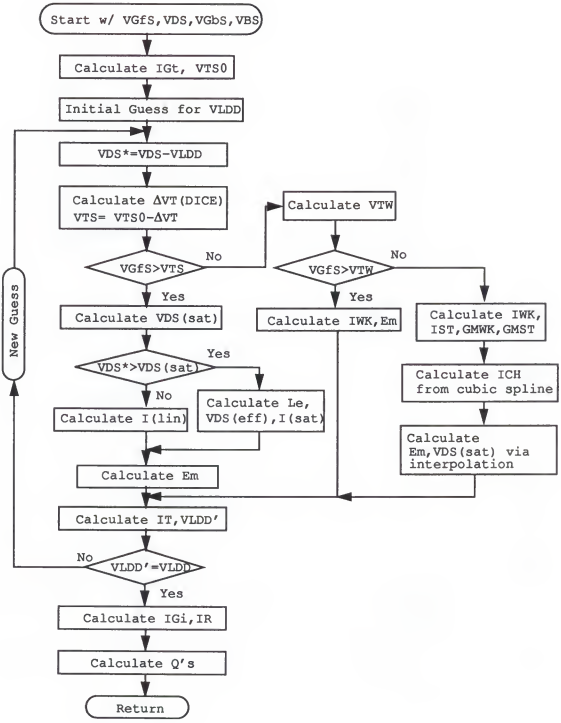


Fig. 4.1 Flowchart of FD/SOI model routine in SOIMOD. Refer to the model network in Fig. 2.2.

into (3.20) to update the back-gate voltage $V_{GbS(eff)}$ and obtain next solution of y_m. These steps are repeated until the convergence requirement is met, which only takes a few iterations.

Fig. 4.2 illustrates the procedure used in calculating the subthreshold current within the loop of Fig. 4.1. First, the back-surface boundary condition is modified iteratively (only one iteration is necessary) by the two-dimensional field in the buried oxide, which gives the effective back-gate bias. Next the effective channel lengths at both front and back surfaces are derived based on the analytic potential solutions from (3.24) and (3.25). The subthreshold current is then given by (3.26), which comprises I_{WKf} and I_{WKb} evaluated by charge partition. In addition, the maximum drain junction-field E_m used for the LDD analysis in weak inversion [Cho91] is approximated by the derived potential solution at y = L as

$$E_m = \frac{\partial}{\partial y}\Psi(x,y)\bigg|_{y=L} - \frac{\partial}{\partial y}\Psi(x,y)\bigg|_{y=L,\,VDS=0} . \tag{4.1}$$

The second term in (4.1) forces the solution for E_m to be consistent with the previously derived drain field under the gate [Cho91] based on the strong-inversion channel length-modulation analysis in [Vee88], in which the electric field is obtained by applying Gauss's law to the portion of channel where the carrier velocity is saturated.

For the device operated in the moderate-inversion region ($V_{TW} < V_{GfS} < V_{TS}$), both currents and their derivatives (with respect to V_{GfS}) need to be calculated at the V_{GfS}

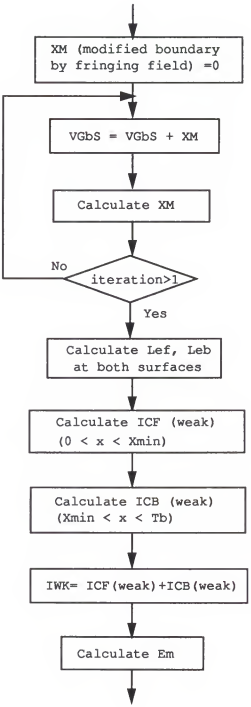


Fig. 4.2 flowchart for calculating subthreshold current.

boundaries to formulate the cubic-polynomial interpolation. Compared to the previous approach utilizing limited (diffusion) current to provide transition between the weak- and strong-inversion region [Cho91], the new moderate-inversion analysis increases the computation time by about factor of two due to additional computations like these, but it outperforms the previous model in terms of physical representation and accuracy. The strong-inversion analysis in Fig. 4.1 is similar to that of the original model routine [Vee88] except the accounting for surface state as illustrated in Chapter 3, and therefore will not be discussed here.

The complete set of 43 model parameters for the n-channel device is listed in Table 4.1, including definitions and default values. Most of model parameters pertain to SOISPICE-2 and are either process or device-physics related. We have added two semi-physical parameters used for the subthreshold fringing-field analysis: GAMMA and KAPPA represent the BOX fringing-field weighting factors; typical values for them with respect to the (back) oxide thickness were given in Table 3.1. KAPPA can be further used to turn off the two-dimensional subthreshold model by setting its value to zero, in which case SOIMOD_3 is called rather than SOIMOD. The value of GAMMA, which replaces the fitting parameter LIMFAC used in the previous model, needs to be set to about 3 to smooth the current transition between weak- and strong-inversion regions [Cho91].

Table 4.1
FD/SOI MOSFET Model Line Parameters

Name	Description	Units	Default
VFBF	Front-gate flatband voltage	V	
VFBB	Back-gate flatband voltage	V	call.
WKF	Front-gate work function difference	V	calc.
WKB	Back-gate work function difference	V	calc.
NQFF	Front oxide fixed charge (normalized)	cm^{-2}	0.0
NQFB	Back oxide fixed charge (normalized)	cm^{-2}	0.0
TOXF	Front-gate oxide thickness	m	1.0
TOXB	Back-gate oxide thickness	m	0.5e-6
NSUB	Substrate doping density	cm^{-3}	1.0e15
NGATE	Poly gate doping density	cm^{-3}	1.0e19
NSF	Front surface state density	$cm^{-2} \cdot eV^{-1}$	0.0
NSB	Back surface state density	$cm^{-2} \cdot eV^{-1}$	0.0
TPG	Type of gate material +1) opposite to body -1) same as body 0) aluminum	-	1.0
TPS	Type of substrate +1) opposite to body -1) same as body	-	-1.0
TB	Film (body) thickness	m	0.1e-6
NBODY	Film (body) doping density	cm^{-3}	5.0e16
UO	Zero field mobility	$cm^2 \cdot V^{-1} \cdot s^{-1}$	700.0
THETA	Mobility degradation coefficient	$cm \cdot V^{-1}$	1.0e-6

Table 4.1 -- continued

Name	Description	Units	Default
BFACT	V_{DS}-averaging factor for mobility degradation	-	0.3
VSAT	Carrier saturated drift velocity	$cm \cdot s^{-1}$	1.0e7
ZETA	On/off flag for charge sharing (0 for no charge sharing)	-	1.0
ALPHA	Impact-ionization parameter a_0 (0 for no impact ionization)	cm^{-1}	0.0
BETA	Impact-ionization parameter b_0 (0 for no impact ionization)	$V \cdot cm^{-1}$	0.0
GAMMA	BOX fringing field weighting factor, or Subthreshold fitting parameter	-	0.3
TAUO	Carrier lifetime in lightly doped region	s	1.0e-6
LLDS	LDS region length (0 for no LDS)	m	0.0
LLDD	LDD region length (0 for no LDD)	m	0.0
NLDS	LDD/LDS doping density	cm^{-3}	3.0e18
NDS	Source/drain doping density	cm^{-3}	5.0e19
JRO	Body-source junction recombination current coefficient	$A \cdot m^{-1}$	1.0e-15
ETA	On/off flag for DICE (0 for no DICE)	-	1.0
LMOD	On/off flag for channel-length modulation	-	1.0

Table 4.1 -- continued

Name	Description	Units	Default
CGFDO	Gate-drain overlap capacitance	$F \cdot m^{-1}$	0.0
CGFSO	Gate-source overlap capacitance	$F \cdot m^{-1}$	0.0
CGFBO	Gate-body overlap capacitance	$F \cdot m^{-1}$	0.0
RHOSD	Source/drain sheet resistance	ohm/sq.	0.0
RHOB	Body sheet resistance	ohm/sq.	0.0
RD	Specific drain parasitic resistance	ohm•m	0.0
RS	Specific source parasitic resistance	ohm•m	0.0
RB	Body parasitic resistance	ohm	0.0
DL	Channel-length reduction	m	0.0
DW	Channel-width reduction	m	0.0
KAPPA	BOX fringing field weighting factor (0 for no fringing)	-	0.5

4.2.2 Modified Source Code from SOISPICE-2

The four-subroutine model structure of SOISPICE-2 [Fos93] is retained in SOI-SPICE-4. The subroutines are SOIFET, SOIID, SOIMOD, and SOIEC. SOIFET processes DC and transient analyses of SOI MOSFETs. It performs the terminal-voltage initialization based on the previous solution, voltage-iterate limiting, and terminal charge integration. It loads the admittance matrix, which includes linearized conductances and current sources, for the SPICE nodal analysis. Called by SOIFET, SOIID calculates the drain currents and terminal charges at the passed operation point for DC and transient modes. It numerically calculates the current and charge derivatives by calling SOIMOD with slightly perturbed values of each of the four terminal voltage differences relative to the source (e.g., V_{GfS}, V_{GbS}, V_{DS}, V_{BS}) in both forward and inverse operations. SOIMOD, the primary model routine, then calculates the different current components, including channel current, thermal generation current, impact-ionization current, and parasitic BJT current, as well as terminal charges for each operating point accessed by SOIID. SOIFET also calls SOIEC during transient (and AC) analysis. SOIEC calculates the equivalent conductances for the intrinsic model, and adds the charge and conductance due to the overlap capacitances to the intrinsic components. All of the device/model parameters and intermediate variables used in the model subroutines are defined or calculated in MODCHK.

The subroutines SOIFET, SOIID, and SOIMOD have been modified to implement the new subthreshold modeling. The

original model routine, with minor upgrades, is renamed SOIMOD_3 for distinction. The main upgrades in SOIMOD, relative to the original model routine are: (1) new weak-inversion current/charge modeling; (2) moderate-inversion accounting with physically defined weak- and strong-inversion boundaries; and (3) accounting for front and back surface-state and substrate depletion charges. SOIMOD_3 provides a user option to access the original FD/SOI model, which is adequate for sub-micron, but not deep-submicron, circuit applications. SOIMOD_3 is upgraded to account for substrate depletion charge under the source/drain region, and surface-state charge as well. SOIID, which calls the model routine to calculate the transistor's current/charge and their derivatives at each bias point, is extended for hierarchy by using KAPPA to access the new subthreshold model in SOIMOD. If KAPPA = 0, then SOIID calls SOIMOD_3. Fig. 4.3 exemplifies the difference between the subthreshold characteristics obtained by SOIMOD and SOIMOD_3 as a function of channel length. It shows that for the long-channel length device (L = 0.5 μm) the simulation results from both models are consistent, except in the transition region due to different interpolation schemes used. As the channel length is scaled down to deep-submicron values however, the two-dimensional formalism implemented in SOIMOD is able to predict the increase of S due to shorter L, which contrasts with ideal S given by SOIMOD_3.

The calculation of extrinsic overlap capacitance between the back gate (substrate) and the source/drain region is commented out in MODCHK since it is now implicitly

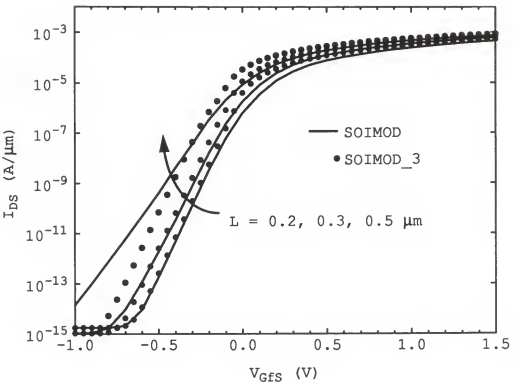


Fig. 4.3 Comparison of n-channel FD/SOI subthreshold characteristics predicted by using SOIMOD and SOIMOD_3 at V_{DS} = 2.5 V; t_{of} = 7 nm, t_b = 50 nm, t_{ob} = 100 nm and $N_A = 5 \times 10^{16}$ cm^{-3}.

included in the substrate-depletion-charge formalisms ((3.55) and (3.56)). Furthermore, the charge-coupling factors α and β defined in MODCHK are modified to account for the influence of surface states on device characteristics (see Chapter. 3). Further the threshold voltages are now defined for both weak and strong inversion; V_{TW} and V_{TS} are added to the state-variable table in SOIFET as device operating-point information.

4.3 PISCES/MEDICI Support

The physical nature of our model enables direct link to the numerical device simulators. The device/model parameters in SOI-SPICE can be effectively defined based on the device structure (e.g., L, TOXF, TOXB, TB), processing information (e.g., NBODY, NGATE, NDS), and physical parameters (e.g., UO, VSAT, TAUO) specified for the two-dimensional numerical device simulator. Unlike empirical SPICE models which require optimization of model parameters by I(V) curve fitting, a direct comparison of the device's I-V characteristics predicted by SOI-SPICE and the numerical device simulator can be obtained.

Model verification is provided by good agreement between the subthreshold characteristics predicted by SOI-SPICE and numerical device simulators (PISCES [TMA89] and MEDICI [MED92]) for a variety of scaled FD/SOI MOSFET structures. Fig. 4.4(a) shows the subthreshold characteristics of a lightly-doped ($N_A = 2x10^{16}$ cm^{-3}) 100-nm-thick n-channel device predicted by PISCES and SOI-SPICE for

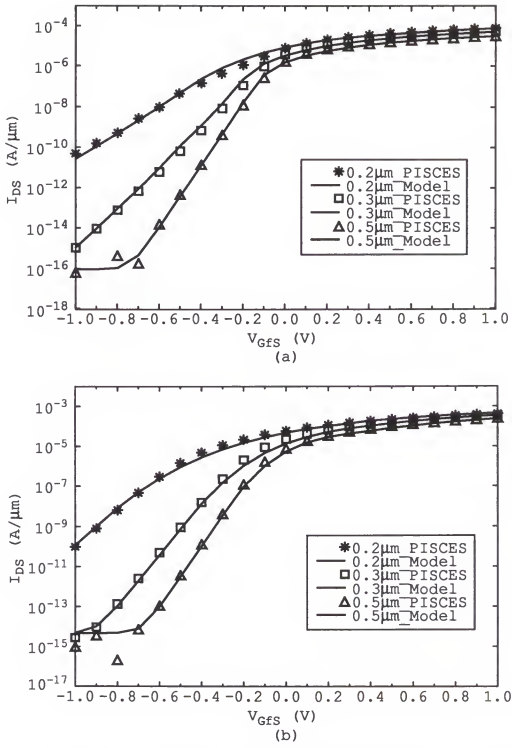


Fig. 4.4 Comparison of model- and PISCES-predicted n-channel FD/SOI MOSFET I_{DS} - V_{GfS} characteristics for different values of L at (a) V_{DS} = 50 mV, t_b = 100 nm (b) V_{DS} = 2.5 V, t_b = 50 nm; N_A = $2x10^{16}$ cm^{-3}, t_{ob} = 350 nm.

different channel lengths at low drain bias (V_{DS} = 50 mV), illustrating the increase of S as L is scaled to deep-submicron lengths. Fig. 4.4(b) shows the predicted characteristics at high drain bias (V_{DS} = 2.5 V), with the film thickness scaled down to 50 nm to avoid punchthrough current, which is not modeled in SOI-SPICE. Comparison of Figs. 4.4(a) and 4.4(b) reveal that the model accounts for drain-induced effects, that is DIBL, well. Moreover, the predicted currents in the moderate-inversion region agree well with the PISCES-simulated results, which can be attributed to our physically based interpolation scheme.

In Fig. 4.5, the back-surface state density (N_{sb} = $2x10^{11}$ $cm^{-2}eV^{-1}$) is included in the simulated 0.2-μm n-channel device at different drain bias; the model-calculated curves fit corresponding MEDICI-simulated data quite well. The influence of surface states on the device threshold voltage and subthreshold swing is also modeled well, as can be seen by comparing result to that obtained without surface state. Fig. 4.6 illustrates the predicted subthreshold characteristics versus body doping density for t_b = 50 nm and L = 0.2 μm at low V_{DS}, suggesting that increasing the film-body doping ($3x10^{17}$ cm^{-3}) effects improvement in S (76 mV) as well as reasonable threshold voltage (0.3 V) by controlling the short-channel effects. Fig. 4.7 shows the predicted drain-induced shift of the subthreshold characteristic for the L = 0.2 μm device with higher N_A ($3x10^{17}$ cm^{-3}) and thinner t_{ob} (100 nm). Note that for this device S is not significantly affected by V_{DS}, and the roll-off of threshold voltage is restricted well. (The good agreement between the

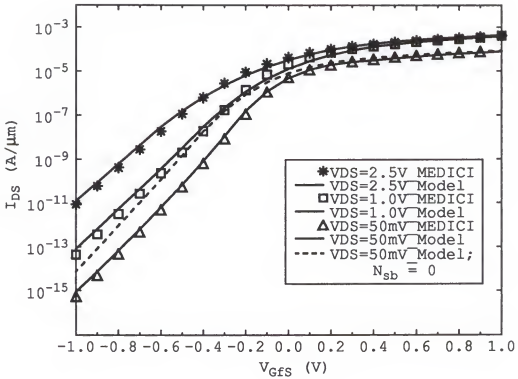


Fig. 4.5 Comparison of model- and MEDIC-predicted n-channel FD/SOI MOSFET I_{DS} - V_{GfS} characteristics for different values of V_{DS}; N_{sb} = $2x10^{11}$ $cm^{-2}eV^{-1}$, L = 0.2 μm, t_b = 50 nm, t_{ob} = 350 nm, and N_A = $2x10^{16}$ cm^{-3}. The dash curve represents the model-predicted current with N_{sb} = 0 at V_{DS}= 50 mV.

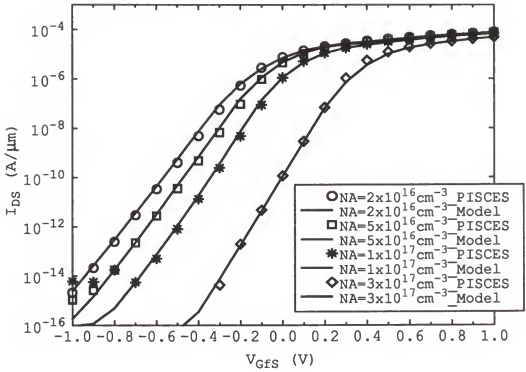


Fig. 4.6 Comparison of model- and PISCES-predicted n-channel FD/SOI MOSFET I_{DS} - V_{GfS} characteristics for different values of N_A at V_{DS} = 50 mV; L = 0.2 μm, t_b = 50 nm, and t_{ob} = 350 nm.

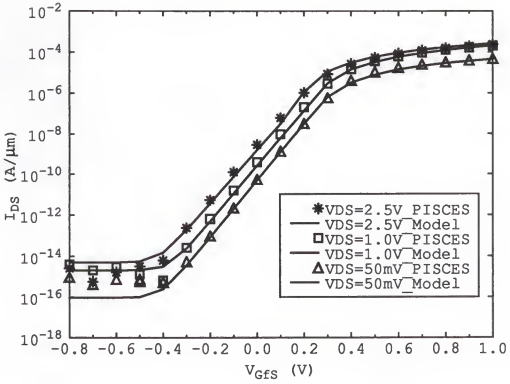


Fig. 4.7 Comparison of model- and PISCES-predicted n-channel FD/SOI MOSFET I_{DS} - V_{Gfs} characteristics for different values of V_{DS}; L = 0.2 μm, t_b = 50 nm, t_{ob} = 100 nm, and N_A = $3x10^{17}$ cm^{-3}.

SOI-SPICE and PISCES predictions for the thinner-t_{ob} device in Fig. 4.7 resulted after increasing the weighting factors γ and κ to 0.9 and 1.0, respectively, as indicated in Table 3.1) These results demonstrate the capability of our physical model in predicting device characteristics, which takes only a small fraction of the run-time required for PISCES/MEDICI simulations, yet provides accurate results.

For all the (floating-body) simulations described above, the insignificance of body charging and V_{BS} with respect to the body potential was ensured by forcing the strongly FD condition previously discussed in Chapter 3. In some cases this condition, as shown by the PISCES simulations, was supported in part by the source/drain charge sharing. Furthermore, the parasitic BJT-induced breakdown or latch was also avoided. Such insurance and avoidance are forced in the FD/SOI CMOS design study in Chapter 5 as well.

4.4 Comparison with Device Measurements

Due to the physical nature of our model, key model parameters can be estimated well based on knowledge of the device structure, and then systematically tuned by measurements at bias conditions which isolate each parameter. To begin this parameter evaluation, we used some structural information directly, for example front-gate/back-gate oxide thicknesses (TOXF, TOXB), and approximated film thickness (TB) as well as body doping (NBODY) based on the technology since TB and NBODY cannot be precisely known.

A set of good initial parameter values is thus defined. Then we systematically tune a smaller set of key parameters. First we examine the measured long-channel subthreshold data at low V_{DS}; if S is non ideal (e.g., > 60 mV), which implies that the back-surface state density (NSB) can be significant, the value of NSB then can be extracted by matching the simulated and measured long-channel subthreshold swing. (It should be noted that TB and NBODY have only second-order effects on S for long L.) Next the fixed oxide charge in the back gate (NQFB) and NBODY are tuned to the measured threshold voltage; a near-perfect front interface is assumed because of the clean thermal oxidation. The low-field mobility (UO), mobility degradation coefficient (THETA), and source/drain series resistances (RS, RD) can then be extracted from strong-inversion I_{DS}-V_{GfS} characteristics at low V_{DS} [Vee88], while the saturation velocity (VSAT) is tuned with V_{DS} close to the saturation voltage. It is noted that the self-heating effect can have significant impact on parameter evaluation, and therefore this tuning should be performed in the low-V_{GfS} saturation region.

For the short-channel device, the impact-ionization coefficients APLHA and BETA are set to 2.45×10^6 and 1.92×10^6, respectively, in accord with the non-local model [Kri93], and the junction recombination current coefficient JRO is varied to match the measured breakdown voltage. The BOX fringing field factors GAMMA and KAPPA are estimated from Table 3.1 for the given TOB. The subthreshold I_{DS}-V_{GfS} characteristics at low-and-high V_{DS} are then used to

determine the lateral diffusion (DL), which mostly affects S. Due to the rigorous subthreshold modeling, DL and TB may need to be tuned iteratively to obtain consistent results; the tuning however does not involve extensive optimization.

Comparison of model predictions with measured I_{DS}-V_{Gfs} data of enhancement-mode n-channel FD/SOI MOSFETs having different channel lengths are presented in Fig. 4.8 at low and high V_{DS}. (The measurement data were acquired from Massachusetts Institute of Technology in collaboration with Professor Dimitri A. Antoniadis.) Key process parameters are t_{of} = 9 nm, t_b = 62 nm, t_{ob} = 380 nm, N_A = 1.5×10^{17} cm^{-3}, and R_{SD} (source-and-drain series resistance) = 30 ohm, with the effective channel length (L) varied from 0.16 to 0.56 μm. Good agreement is obtained in most operation regions. We note in Fig. 4.8 (b) evidence of kinks in the subthreshold region of the longer-channel devices at high V_{DS}. We suspect that the reason is because the bodies of these devices are not strongly depleted; therefore the impact ionization-injected holes perturb the back surface potential and increase the front-channel current through charge coupling [Kri95]. A discrepancy also occurs in the subthreshold region of the 0.16-μm device in Fig. 4.8(a), which we attribute to punchthrough evidenced by loss gate control in the actual device. The key extracted model parameters are listed in Table 4.2, which correlate well with the given process information. It is interesting to note that the extracted back-surface state density, which is about 1.5×10^{11} $cm^{-2}eV^{-1}$, is consistent with published SOI data for thick back-gate oxides [Che92].

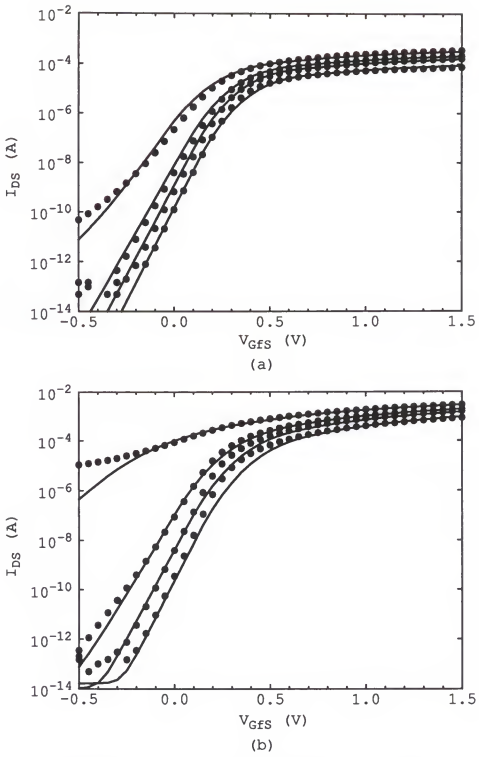


Fig. 4.8 Measured (dot) and simulated (solid) I_{DS}-V_{GfS} characteristics for L = 0.16, 0.26, 0.36, 0.56 μm at (a) V_{DS} = 50 mV and (b) V_{DS} = 1.55 V; W = 10 μm. Note in (b) the evidence of subthreshold kinks for L = 0.36, 0.56 μm.

Table 4.2
LIST OF EXTRACTED PARAMETERS

Parameter	Extracted Value
NSB	1.5×10^{11} $cm^{-1} \cdot eV^{-1}$
NQFB	$< 2 \times 10^{10}$ cm^{-2}
NBODY	1.6×10^{17} cm^{-3}
TB	60 nm
UO	510 $cm^2 \cdot V^{-1} \cdot s^{-1}$
THETA	2.0×10^{-6} $cm \cdot V^{-1}$
RS/RD	155×10^{-6} ohm•m
VSAT	8×10^6 $cm \cdot s^{-1}$
GAMMA	0.3
KAPPA	0.5

With the same evaluated parameters, we also compare the simulated and measured output characteristics. Fig. 4.9 plots the I_{DS}-V_{DS} characteristics of a 0.26-μm n-channel FD/SOI MOSFET at constant $V_{GFS} - V_{TH}$, where V_{TH} is the linearly-extrapolated threshold voltage at low V_{DS}. The breakdown characteristic at low V_{GfS} is matched well by tuning the value of JRO to 2.5×10^{-16} $A\text{-}m^{-1}$. The comparison shows a significant discrepancy in the high-V_{GfS} saturation region, which we attribute to the self-heating effect under high static power dissipation not accounted for in our model.

4.5 Summary

In this chapter, the implementation of our newly developed subthreshold model into the SOI-SPICE circuit simulator was described. Due to the physical nature of the model, an efficient parameter-evaluation algorithm can be defined based on the device structure, involving eased parameter tuning. The new subthreshold model was verified based on numerical device simulations as well as device measurements, and was shown to be predictive for deep-submicron devices, without requiring empirical fitting. The new model facilitates examination of the scaling of FD/SOI in a systematic way with afforded insights. Its capability in performing device/circuit simulations in an easy and efficient way is a real advantage over two-dimensional device simulators, which are much more intensive (and even equivocal due to physical modeling deficiencies).

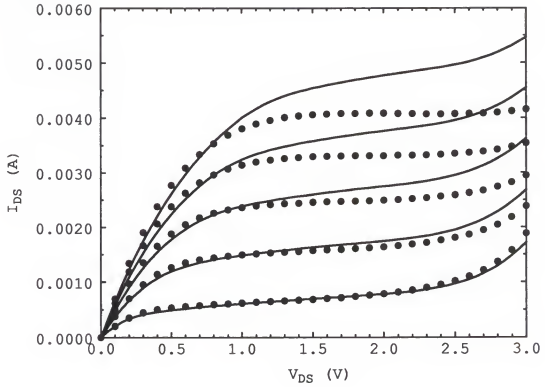


Fig. 4.9 Measured (dot) and simulated (solid) I_{DS}-V_{DS} characteristics for an L = 0.26 μm n-channel FD/SOI MOSFET at $V_{GS} - V_{TH}$ = 0.5, 1.0, 1.5, 2.0, and 2.5 V; W = 10 μm.

CHAPTER 5
DESIGN AND PERFORMANCE CONSIDERATIONS FOR SCALED FULLY DEPLETED SOI CMOS IN LOW-VOLTAGE APPLICATIONS

5.1 Introduction

Current interest in SOI is focused mainly on low-voltage/low-power digital CMOS applications requiring deep-submicron devices. For low-voltage operation, thin-film fully depleted (FD) SOI MOSFETs are potentially superior to their partially depleted (PD) counterparts in several regards [Fos93], for example, nearly ideal subthreshold slope, immunity to the floating-body kink effect (i.e., threshold reduction), and easily reduced short-channel effect, all of which enable, in principal, scaling of the threshold voltage for speed retention. However, in addition to the deterioration of the subthreshold characteristics due to source/drain field fringing in the back-gate oxide (BOX) studied in Chapters 3 and 4, there is concern also about the sensitivity of the FD/SOI MOSFET threshold voltage to the film thickness since the film must be very thin to assure the FD condition [Hwa93]. Conversely the PD/SOI MOSFET, whose threshold voltage depends on maximum depletion depth under the front gate, offers better threshold voltage control [Sha93].

In Section 5.2, we use our developed subthreshold model to gain insight regarding design of deep-submicron FD/SOI

CMOS for low-voltage applications. The design first shows that a thin BOX tends to suppress the two-dimensional field fringing at the back surface, and thereby reduce the leakage current. Although thinning the BOX implies increasing source/drain (to substrate) capacitance, the high-resistivity substrate commonly used in SOI technology becomes depleted and effectively limits the capacitance [All93]. Furthermore, the source/drain charge-sharing effect is found to decrease the threshold-voltage variation with respect to the film thickness in the scaled device, and hence possibly improves VLSI circuit manufacturability.

Our design study suggests that the performance of conventional FD/SOI is attractive for quarter-micron digital CMOS applications, but the advantages rapidly disappear as the channel length is shrunk to the 0.1-μm regime due to weak front-gate control of the back surface. We show in Section 5.3 by two-dimensional numerical simulations that scaling the BOX with subsequent substrate engineering is required for improving the short-channel effects, which are further complicated by a subthreshold kink effect [Kri95]. In Section 5.4 the scaling capability of FD/SOI is evaluated by SOI-SPICE with afforded physical insight. The simulation results suggest a need for innovation for viable FD/SOI technology in the future.

5.2 Viable Quarter-Micron SOI CMOS Design

To exemplify the utility of new subthreshold model in SOI-SPICE-4, we use it to define a viable design for quarter-

micron (effective L = 0.2 μm) FD/SOI CMOS technology based on simulated speed and static power in low-voltage digital circuits. Low-dose SIMOX material with thin BOX (t_{ob} = 100 nm) is used in this design to reduce the leakage current by suppressing the field fringing. Fig. 5.1 plots the SOI-SPICE-predicted I_{DS}-V_{GfS} characteristics of a 0.2 μm n-channel FD/SOI MOSFET with different values of BOX thickness. It shows that the leakage current is reduced by over an order of magnitude when scaling the BOX from 400 nm to 100 nm (provided substrate depletion under the channel is negligible).

Thin BOX also increases thermal conductivity (reduces self heating) and expedites material (SIMOX) production. Although thin t_{ob} means high BOX capacitance, the implied increase of the (NMOS) source/drain capacitance can be offset by the use of high-resistivity (p-type) substrate. For example, Fig. 5.2 shows plots of the calculated effective source/drain capacitance ($C_{S/D}$), which is defined by the series combination of the BOX capacitance (C_{ob}) and the substrate depletion capacitance (C_{dep}), as a function of BOX thickness for different substrate doping. Here 2.5 V is applied to the source/drain-to-substrate capacitance. The increase of source/drain capacitance for the lightly doped substrate (N_{sub} = $1x10^{15}$ cm^{-3}) is found to be negligible when t_{ob} is scaled from 350 nm to 100 nm, which contrasts with the results from using heavily-doped substrate (N_{sub} = $1x10^{17}$ cm^{-3}). Use of thin t_{ob} however is found to produce excessive leakage current in the PMOS device because of enhanced back-gate coupling amplified by V_{GbS} = $-V_{DD}$ (supply voltage) in

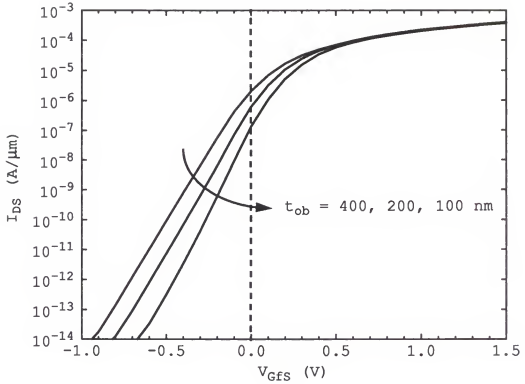


Fig. 5.1 SOI-SPICE-predicted I_{DS} - V_{GfS} characteristics of a n-channel FD/SOI MOSFET for different values of BOX thickness; L = 0.2 μm, t_b = 50 nm, N_A = $2x10^{17}$ cm^{-3}; V_{DS} = 2.5 V.

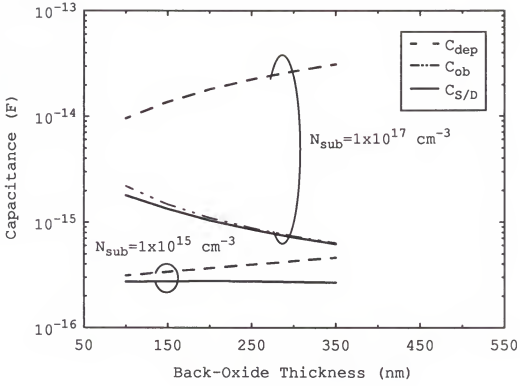


Fig. 5.2 Calculated source/drain capacitance ($C_{S/D}$), (back) oxide capacitance (C_{ob}), and substrate depletion capacitance (C_{dep}) as a function of back-oxide thickness. The capacitance area is 6.6 pm^2.

CMOS circuits. Several design alternatives, for example, n^+ poly gates or hybrid FD/PD CMOS, for controlling PMOS leakage but retaining NMOS performance are assessed by SOI-SPICE-4, identifying the viable design and required tradeoff for the deep-submicron FD/SOI CMOS technology.

5.2.1 Preliminary Design

Table 5.1 describes a preliminary (enhancement-mode) FD/SOI CMOS design using dual-poly gates, which was evolved from copious n-channel device simulations exemplified in Chapter 4, and summarizes key NMOS and PMOS characteristics predicted by SOI-SPICE-4. The design presumes 0.2-μm effective channel lengths, dual poly gates, and a 2.5 V supply voltage. We have accounted for the fixed oxide charges and surface states of the SOI film, which can be significant especially at the back silicon/oxide interface due to oxygen-implantation damage. The surface-state charging tends to deteriorate the subthreshold slope as indicated in Fig. 4.5 due to the reduced front-channel control. (The values of the fixed charges and surface state densities are extracted from current technology and assumed independent of oxide thickness.)

For deep-submicron devices, high film-body doping is required for acceptable threshold voltage and control of source/drain charge-sharing effects. Hence the film thickness must be thin to ensure the FD condition. We stress however that the encroachment of the source/drain junction fields under the gate partially supports the FD condition,

Table 5.1
Preliminary FD/SOI CMOS Design

	n-channel	p-channel
L (μm)	0.2	
W(μm)	3.3	6.6
$t_{of}/t_b/t_{ob}$ (nm)	7/50/100	
N_A, N_D (cm^{-3})	$3x10^{17}$	
N_{Qff}/N_{Qfb} (cm^{-2})	$1x10^{10}/1x10^{11}$	
N_{sf}/N_{sb} (cm^{-2}/eV)	$2x10^{10}/2x10^{11}$	
N_{SUB} (cm^{-3}, p-type)	$1x10^{15}$	
μ_0 ($cm^2/V-s$)	400	210
R_{SD} (Ω)	60	
V_T (V)	0.39	-0.25
I_{leak} (nA/mm @ 2.5V)	1.0	15.0
S (mV)	74	75
I_{on}/I_{leak} (@ 2.5V)	$5x10^5$	$3.3x10^4$

thereby diminishing the sensitivity of threshold to t_b, which in contrast is exclusively controlled by the front gate-back gate charge coupling in the long-channel FD device. Fig. 5.3 shows SOI-SPICE-predicted sensitivities of the n-channel FD/SOI threshold voltage and leakage current to ±10% variations of film thickness and channel length from their nominal values (the threshold voltage is defined as the front gate voltage at which $|I_{DS}| = 0.1(W/L)$ μA at $|V_{DS}| = 50$ mV). Contrary to the results of analyses of long-channel devices [Sme93], we see that the sensitivity of the threshold voltage (5.6 mV/nm), as well as the leakage current, to t_b is not significant in this scaled device. The sensitivities of the threshold and leakage current to L are also tolerable due to the reduced short-channel effect afforded by thinning t_b and t_{ob}.

Fig 5.4 shows the predicted subthreshold characteristics of the designed CMOS devices with different back oxide thicknesses. For the n-channel device, scaling t_{ob} from 350 nm to 100 nm, as we have done, is able to reduce the leakage current by an order of magnitude because of suppressed field-fringing in the BOX. However, for the p-channel device, which is typically subjected to negative back-gate (substrate) bias (relative to the source) in a CMOS circuit, there is an increase of leakage current due to the enhanced back-channel conduction as indicated by an increase of S, which further couples to the front surface and reduces the threshold voltage.

These preliminary results show that our conventional design (in Table 5.1) is inadequate for L = 0.2 μm, but they

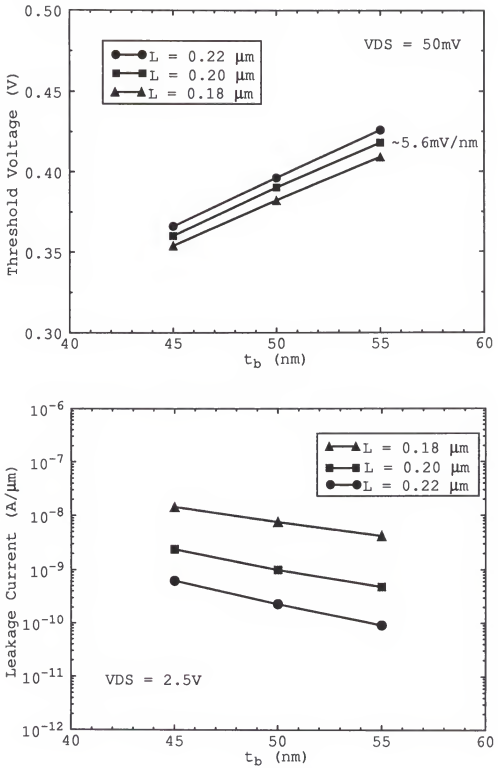


Fig. 5.3 SOI-SPICE-predicted threshold voltage and leakage current versus ±10% variations in FD/SOI film thickness and channel length.

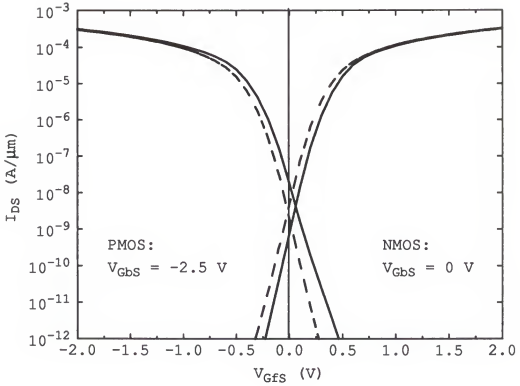


Fig. 5.4 SOI-SPICE-predicted subthreshold characteristics for dual-poly CMOS devices (Table 5.1) with t_{ob} = 350 nm (dashed curves) and t_{ob} = 100 nm (solid curves).

indicate that a conventional dual-poly-gate design can be viable for slightly longer effective channel length, for example, L ≈ 0.25 μm [Kad95].

5.2.2 n+ Poly-Gate Alternative

Intuitively, the p-channel leakage can be suppressed by using different gate material, for example, n^+ polysilicon. The reduced front-gate work function enables the channel doping (N_D) to be lower than that for the previous p^+-poly design for acceptable on-state current, yet it must be high enough to restrain excessive leakage current.

We simulate an unloaded four-stage n^+ poly-gate CMOS inverter circuit operating at V_{DD} = 2.5 V using CMOS structures described in Table 5.1 but lower N_D ($2x10^{16}$ cm^{-3}) for the p-channel device. The SOI-SPICE-predicted gate propagation delay plotted in Fig. 5.5(a) versus t_{ob} shows little speed degradation as the back-oxide thickness is scaled down. The predicted delay for abnormally high substrate doping (N_{sub} = $1x10^{19}$ cm^{-3}) is plotted to reveal the benefit of the mentioned substrate depletion. Also plotted in Fig. 5.5(a) is the delay predicted when dual-poly gates are used. Note (for V_{DD} = 2.5 V) that use of only n^+ poly gates does not significantly sacrifice speed compared to that for dual-poly gates (15 - 20% degradation); yet results in much less static power consumption as shown by the simulation results presented in Fig. 5.5(b). These results suggest that static power, not speed, defines the lower limit (t_{ob} ≅ 100 nm) of BOX thickness. This limit is imposed

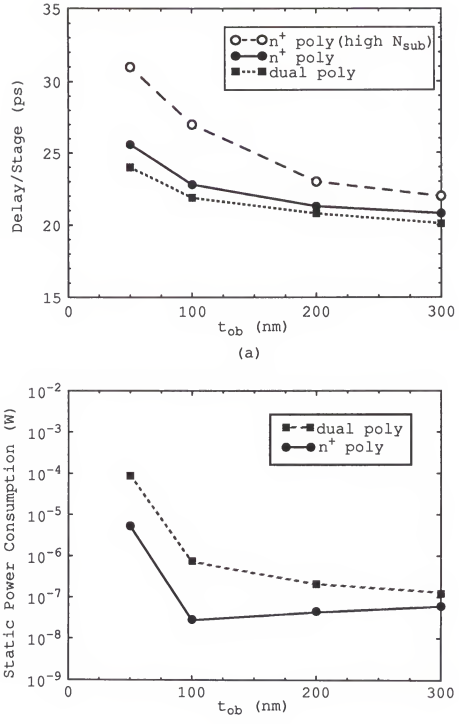


Fig. 5.5 SOI-SPICE-predicted (four-stage) FD/SOI CMOS inverter (a) gate propagation delay and (b) static power consumption versus t_{ob} for different gate materials; L = 0.2 μm, V_{DD} = 2.5 V.

by the lowering of the PMOS threshold voltage via charge coupling between the front and back gates, which is enhanced as t_{ob} decreases. The simulations reveal that for thicker t_{ob} the NMOS leakage current, which flows predominantly along the back surface, is predominant, and is reduced as t_{ob} is scaled because of suppressed field fringing. For $t_{ob} < 100$ nm however, the charge coupling is intensified and the PMOS front-channel current becomes the predominant leakage component.

For lower V_{DD} (< 1.5 V as in battery-operated circuits), the n^+ poly-gate technology is unacceptable for FD/SOI CMOS. Fig. 5.6 shows the propagation delay and static power versus V_{DD} predicted by SOI-SPICE simulations of the FD/SOI CMOS circuits for n^+ and dual-poly gates, including effects of ±10% variations in t_b, which are small. Because of the limited PMOS current drive, the n^+ poly gates do not appear viable for $V_{DD} < 2$ V. The dual-poly technology retains speed performance, but with relatively high static power due to PMOS leakage current.

5.2.3 Hybrid CMOS Alternative

Another means of reducing PMOS leakage is to design for a partially depleted (PD) condition in the p-channel device, thereby eliminating the charge coupling to the back gate, which underlies the excessive leakage current. The FD NMOS can be retained to exploit its benefits, for example, suppression of floating-body effects [Suh95], thus defining "hybrid" design for SOI CMOS. Technically, PD PMOS can be

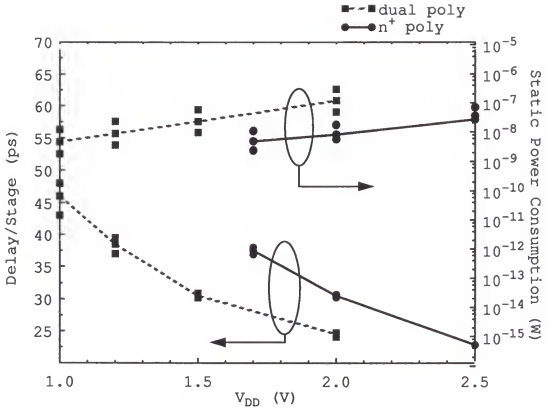


Fig. 5.6 SOI-SPICE-predicted (four-stage) FD/SOI CMOS inverter performance versus supply voltage, including ±10% variations in SOI film thickness; t_{ob} = 100 nm.

fabricated by implementing a higher density of dopants (e.g., Antimony) near the back interface, while retaining lower (effective) channel doping (e.g., Phosphorous) in the channel region. Fig. 5.7 illustrates a typical concentration profile in a processed device versus an ideal (abrupt) one assumed in the PD modeling [Suh95]. The first shallow Phosphorous implant adjusts the front channel threshold voltage, while the second deeper Antimony implant give the back channel high enough threshold voltage to avoid depletion. Such retrograded-channel doping has been employed in bulk CMOS to suppress the punch-through current [Shah93]. It is noteworthy that the impact ionization-induced kink effect is not so significant in PD PMOS due to the reduced hole impact-ionization rate. However, to properly achieve the necessary retrograded doping profile, a relatively thick SOI film is required, which will limit the scaling capability of the FD NMOS built on same wafer. SUPREM-3 [Tma94] simulations of the PD PMOS process show that a film thickness of at least 70 nm is necessary to obtain a front-surface channel doping of about 2×10^{17} cm^{-3} with a retrograde up to about 2×10^{18} cm^{-3} at about 50 nm.

We use SOI-SPICE to examine the performance of hybrid CMOS devices and circuits, accessing now the PD model [Suh95] in SOI-SPICE as well as an upgraded FD model. The designed hybrid CMOS is now built on 70-nm SOI film with 50-nm (depleted) channel thickness (T_B) under the front gate of the p-channel device. The body doping for n- and p-channel devices are 2.5×10^{17} and 2×10^{17} cm^{-3}, respectively. The predicted leakage current-versus-drive current for dual-poly

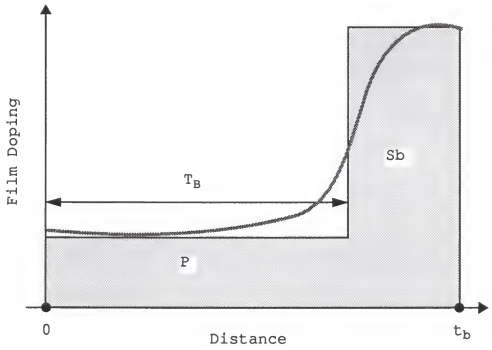


Fig. 5.7 Ideal channel profile (shaded area) of a PD PMOS device; the grey solid-line represent the actual profile after annealing. T_B is the effective (depleted) channel thickness [Suh95].

FD and hybrid FD/PD technologies plotted in Fig. 5.8(a) indicates that this design is viable. The leakage current of the PD/PMOS is diminished dramatically compared to its FD counterpart, and the FD NMOS performance is not sacrificed. Fig. 5.8(b) shows the static power consumption of a four-stage SOI CMOS inverter versus delay for both technologies. Obviously for the same delay, use of hybrid FD/PD SOI is able to consume less static power than FD/SOI for various supply voltages. For example at V_{DD} = 2.0 V, the inverter circuit using the hybrid design dissipates ~10^{-8} W in the standby mode, which is 1/10 that of FD circuit, and its delay of 22 ps/stage is comparable.

Finally, Fig. 5.9 compares the variation of delay time with supply voltage for a two-input NAND, 19-stage ring oscillator predicted by SOI-SPICE. By using the hybrid design, the delay time is 50 ps/stage at V_{DD} = 1.2 V, which is much superior to that of the previously described n^+ poly (175 ps/stage) and is comparable to the dual-poly FD CMOS performance. For comparison, the measured delay by Tsuchiya et al. [Tsu94] of a 0.24- μm (effective L = 0.2 μm) ring oscillator using a comparable dual-poly FD/SOI technology is plotted. Good simulation-measurement agreement is achieved without fine tuning the SOI-SPICE FD model parameters.

The non-scalable film imposed by the hybrid structure however would restrict circuit performance (e.g., static power consumption) as the technology (i.e., L) is reduced. Furthermore, the transient floating-body effect on the threshold voltage of the PD device [Suh95] can lead to circuit instability, and hence complicates design (whereas

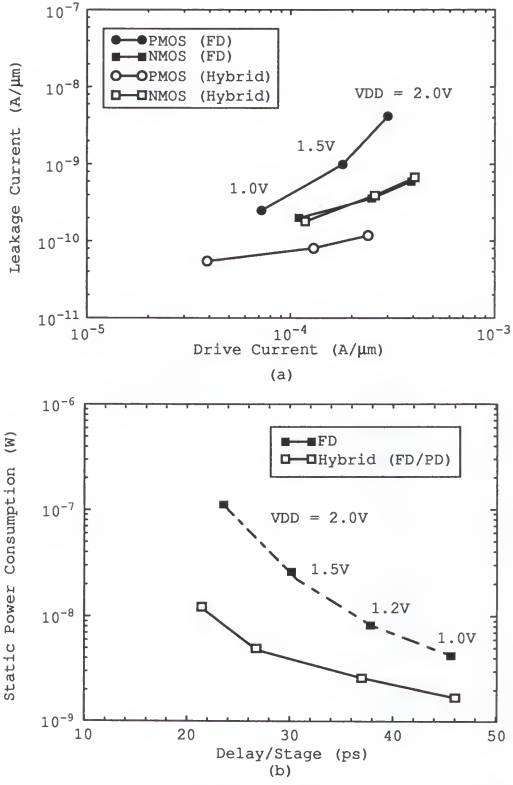


Fig. 5.8 SOI-SPICE-predicted (a) CMOS performances and (b) 4-stage-inverter static power consumption versa delay of both FD/SOI and hybrid FD/PD technologies in different supply voltages.

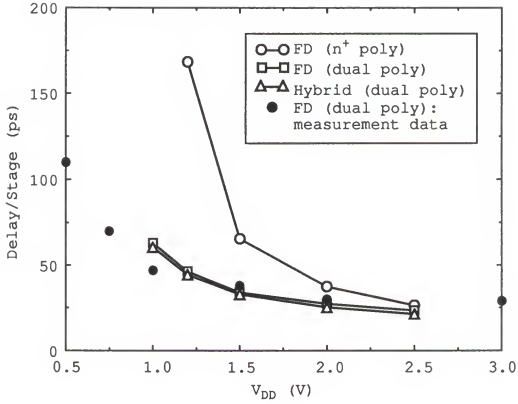


Fig. 5.9 SOI-SPICE-predicted gate delay for a 0.2-μm 19-stage ring oscillator versus supply voltage for different technologies.

FD NMOS remains dynamically stable due to its fully depleted body [Tsu94]). Obviously certain performance tradeoffs need to be assessed in terms of circuit applications.

5.3 Design Complications for Highly Scaled FD/SOI

As the FD device's dimension is scaled to ultra deep-submicron length ($L \rightarrow 0.1$ μm), the required control of the short-channel effects implies thinning down the film and back oxide thicknesses, but increasing the film-body doping to obtain acceptable threshold voltage. Such high doping implies that the device may not be strongly depleted in the subthreshold region, and therefore a floating-body kink effect can occur [Kri95]. In addition, the depleted substrate under the channel region [Joa95] enhances the fringing field as the buried oxide is scaled, negating the advantage of thin BOX in reducing the leakage current. Both of these effects, which previously seemed insignificant and were not accounted for in our FD model, jeopardize the viability of the FD/SOI technology by closing the design window.

5.3.1 Subthreshold Kink Effect

Thin film FD/SOI has been thought to be free of floating-body effects because of the fully depleted body [Cho91]. As the device's dimension is scaled down though, a floating-body kink effect becomes significant in the subthreshold region [Kri95]. Fig. 5.10 shows the measured

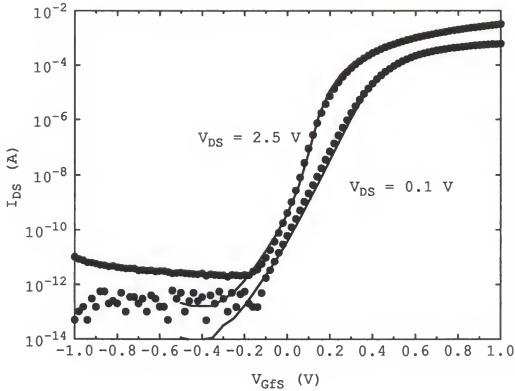


Fig. 5.10 Measured (dot) and MEDICI-simulated (solid curves) subthreshold characteristics of LETI device with different drain bias. L_{eff} = 0.2 μm, W = 10 μm.

subthreshold characteristics of an enhancement-mode, deep-submicron (L_{eff} = 0.2 μm), heavily doped (N_A = $9x10^{17}$ cm^{-3}), and ultra thin (t_b = 30 nm) SOI MOSFET fabricated at LETI with LDDs. (The measurement data were acquired from Laboratory Electronic of Technology and Instrumentation in collaboration with Dr. Olivier Faynot.) The device is classically FD mode because (1) it exhibits near-ideal subthreshold swing (S = 61 mV/dec) at low drain bias as evidenced in Fig. 5.10, and (2) it reflects strong coupling between the front and back gates in the linear region. This device also has a low leakage (0.1 nA/μm) and reasonable threshold voltage (0.35 V) adequate for low-voltage operations. However, we observe in Fig. 5.10 a subthreshold kink in the subthreshold region at high V_{DS}. The reason for this kink can be explained as follows. The device interested is not strongly depleted ($p = n \cong 0$) in the subthreshold region due to its heavily doped film. Since the body is floating, holes generated by impact ionization cause a quasi-Fermi-level separation at the body-source junction, which perturbs the back-surface potential (Ψ_{sb}) two-dimensionally and results in an increase ($\Delta\Psi_{sb} = V_{BS}$) of the potential. The corresponding increase of the front-surface potential via charge coupling therefore increases the subthreshold current and forms the kink. Note that only if the body is strongly depleted will the injected holes make a negligible effect on Ψ_{sb}.

The occurrence of a subthreshold kink in the FD/SOI MOSFET portends dynamic floating-body effects as in PD/SOI MOSFET devices and circuits [Suh95]. However numerical

device simulations with MEDICI, fitted to the LETI device (N_A = $9x10^{17}$ cm^{-3}) by tuning the impact-ionization coefficients (see Fig. 5.10), suggests that the transient threshold voltage resulting from $V_{GfS}(t)$-induced body charging is negligible as exemplified in Fig. 5.11. Included is the simulation result of a device with higher body doping (N_A = $1.5x10^{18}$ cm^{-3}), which shows a transient current overshoot in the on-state and transient current undershoot in the off-state relative to the respective steady-state currents. This higher-N_A device is PD. The simulations reveal that as long as there is no neutral region in the body, irrespective of the degree of depletion and prevalent subthreshold kink, the fluctuation of body charge is minimal and will not perturb the body potential, which is consistent with our fixed body-charge model formalism, and suggests that the FD/SOI CMOS inverter circuit tends to be free of dynamic instability. (We stress that for memory circuits, the FD pass transistor can actually be accumulated during switching, which would cause the transient floating-body effect to materialize. A body contact might therefore be necessary for pass transistors.)

The subthreshold kink can result in significant leakage current if it occurs at the zero front gate-voltage, which would be prohibitive for low-voltage applications. For example, in Fig. 5.12 we use MEDICI to simulate the scaled version (effective L = 0.15 μm) of the LETI device in the subthreshold region at V_{DS} = 1.5 V, showing the increased leakage current at V_{GfS} = 0 V caused by the kink. To suppress the subthreshold kink, we can reduce the body doping and/or

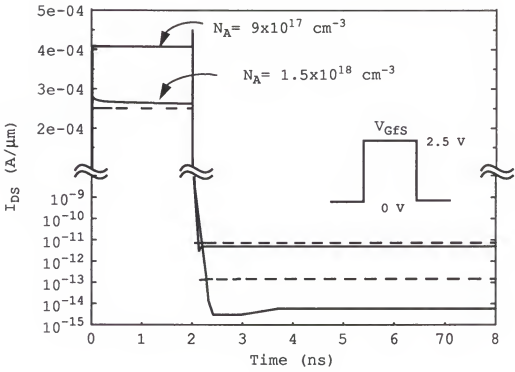


Fig. 5.11 MEDICI-simulated transient drain current (solid curves) resulting from the front-gate turn-on and turn-off pulse with different body doping. The dash curves represent the steady on- and off-currents. V_{DS} = 2.5 V.

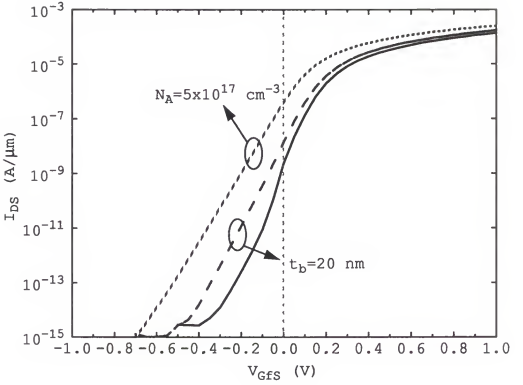


Fig. 5.12 MEDICI-simulated subthreshold characteristics of a scaled version of LETI device (L_{eff} = 0.15 μm, t_b = 30 nm, N_A = 9x10^{17} cm^{-3}) at V_{DS} = 1.5 V. Also plotted are the devices with same structure but having either lower body doping or thinner film to suppress the kink.

scale down the film thickness to yield a strongly FD condition. (Thinner BOX is not effective in this aggressively scaled design.) However, lower body doping also enhances the source/drain charge-sharing and short-channel effect; thinner film improves the short-channel effect but reduces the threshold voltage through the depleted body. Both design options eliminate the kink, but increase the leakage current as evidenced by Fig. 5.12. The balance between kink and charge sharing in minimizing leakage current unfortunately reduces the design flexibility for high-performance FD/SOI CMOS.

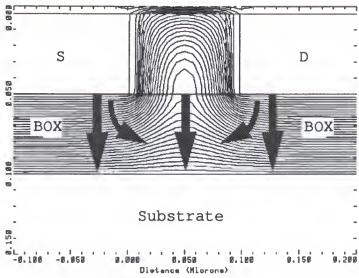
5.3.2 Back-Gate Depletion Effect

Previously we have assumed that the back gate (silicon substrate) remains neutral for all bias conditions and can be modeled as metal. As the back-gate oxide thickness is thinned down to suppress the fringing fields in the scaled device though, depending on the work-function difference between the substrate and the film body as well as biasing, the high-resistivity (p-type) substrate underneath the film body can be depleted. The depletion region can be further facilitated by the encroachment of source/drain junction fields. The resulting potential along the back silicon/oxide interface perturbs the field distribution in the oxide and enhances the influence of source/drain fringing fields on the back channel.

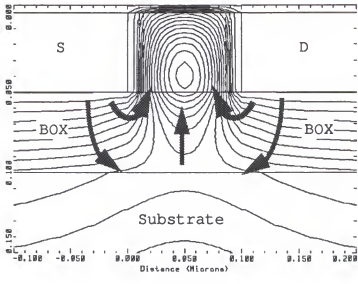
To understand the underlying physical mechanism, two-dimensional simulations using MEDICI are performed on an FD/

SOI structure with 0.1-μm gate length and a 50-nm BOX. The simulated potential contours and interpolated field vectors in the oxide are presented in Fig. 5.13 for two values of substrate doping (N_{sub}). As shown in Fig. 5.13(a) when the substrate is heavily doped and not depleted, an almost uniform field along the back silicon/oxide interface is obtained, and the source/drain field fringing is well controlled. However if the common lightly doped silicon substrate is used in the simulation, the substrate is depleted as shown in Fig. 5.13(b). The depletion charge is supported by the field in the BOX as well as by the quasi-two-dimensional fields underneath the source/drain region. The field lines emanating from the junctions terminate now at the back surface of the SOI film instead of the back gate, reflecting how the potential in the substrate reduces that (Ψ_{sb}) at the back interface.

The influence of back-gate depletion on the device performance is indicated in Fig. 5.14 where the MEDICI-predicted leakage currents of a 0.2-μm n-channel device versus the oxide thickness for different substrate doping are plotted. Apparently scaling t_{ob} does not effectively reduce the leakage current of the device with lightly doped (p-type) substrate ($N_{sub} = 1x10^{15}$ cm^{-3}). (In some devices, the channel dopant atoms (e.g., Boron) can be forced into the substrate to reduce the depletion, especially if t_{ob} is very thin. The benefit is limited by implantation dose and energy however.) The simulation shows that for the device having high substrate doping ($N_{sub} = 1x10^{19}$ cm^{-3}), the leakage current is decreased from 15 nA/μm to 0.21 nA/μm as t_{ob} is



(a)



(b)

Fig. 5.13 MEDICI-simulated equal potential contours and interpolated field vectors for a 0.1 μm n-channel SOI MOSFET biased at $V_{GfS} = V_{GbS} = V_{DS} = 0$ V with different substrate doping. In (a) $N_{sub} = 1x10^{18}$ cm^{-3}; in (b) $N_{sub} = 1x10^{15}$ cm^{-3}.

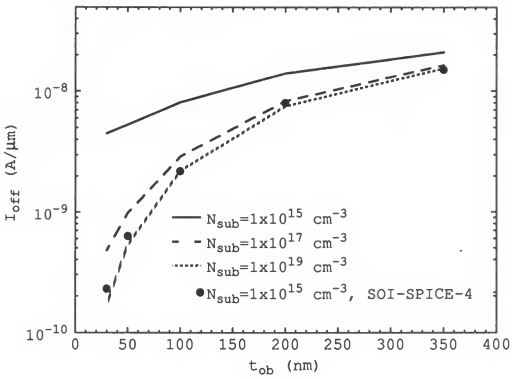


Fig. 5.14 MEDICI- and SOI-SPICE-simulated leakage current (I_{off}) versus t_{ob} for different substrate doping (N_{sub}) at V_{DS} = 2.5 V; L = 0.2 μm, t_b = 50 nm, and N_A = 3x10^{17} cm^{-3}.

scaled from 350 nm to 30 nm. The SOI-SPICE-predicted leakage is plotted in Fig. 5.14 as well. It shows good agreement with the MEDICI-simulated results for high substrate doping since the substrate depletion effect (under the film body) is not accounted for in our model.

The study hence suggests increasing the substrate doping under the channel region for reduced field fringing, while maintaining low-doped substrate under the source/drain region for low capacitance. Plotted in Fig. 5.15 is a cross-sectional view of a SIMOX CMOS structure fabricated by such selective substrate doping [Joa95]. A deep p^+ implantation is performed locally to increase the substrate doping under the NMOS channel region. Additionally a similar n^+ implantation is done under the PMOS device to increase the back-channel threshold voltage and reduce the back gate charge-coupling effects. As indicated in Fig. 5.15, the device fabrication necessitates two additional masks and high energy implantation. It also requires careful temperature control for reducing lateral diffusion of implanted dopants during thermal cycles. These added requirements complicate the design flow and increase the process cost, which may not be practical.

5.4 Optimal Scaling for Deep-Submicron FD/SOI

With the design limitations discussed so far, it becomes questionable whether thin-film FD/SOI technology can be scalable for next-generation CMOS. Several researchers have examined the scaling methodology for thin-film FD/SOI,

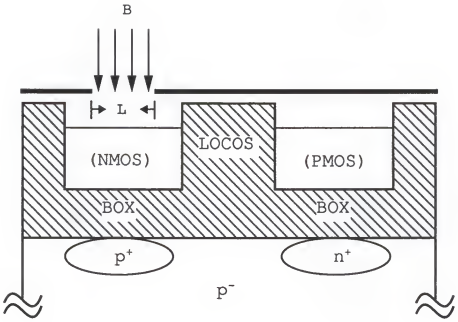


Fig. 5.15 A Cross-sectional view of a SIMOX wafer with the selective implanted substrate.

and suggested that thin film and high body doping are needed for the future scaling. Their approaches, which were mostly based on analytical derivation or two-dimensional numerical device simulations, may not be adequate. For example, Yan et al. proposed a natural-length scaling rule based on simplified two-dimensional Poisson's equation potential solution at the front oxide/silicon interface [Yan92]. The key assumption in their analysis is ignoring the (fringing) field in the buried oxide, which excludes the back-channel conduction as well as front-gate/back-gate charge coupling. Su et al. used two-dimensional numerical simulations to examine the threshold-voltage shift due to charge-sharing and DIBL effects, and defined an optimal design space for varying the device structure in 0.2-μm and 0.1-μm technologies [Su93]. It is however more practical to examine device performance (e.g., saturation current, leakage current, and subthreshold swing) instead of threshold because the threshold voltage is loosely defined and its value depends strongly on the extrapolation scheme used to evaluate it. The resulting inconsistency can become problematic in deep-submicron design with low supply voltage. Furthermore, the long-channel behavior, which is the objective in the threshold-voltage-based design, need not be preserved as long as device characteristics meet the circuit specifications. Finally, the effects of kink and back-gate depletion were both overlooked in [Yan92] and [Su93].

As a precursor to our scaling study, we note that another type of thin-film device has been proposed. The

accumulation-mode (AM) SOI MOSFET [Col91] is fully depleted when the device is turned off, while the front surface is accumulated when the device is turned on. AM SOI CMOS therefore can be realized by using the p^+-poly gate for the NMOS with n-type body doping, and n^+-poly gate for the PMOS with p-type body doping. The main advantages of AM devices are the enhanced current drive due to the addition of bulk current flowing through the neutral region below the accumulated surface, and a good threshold voltage control [Col91]. There is also a flexibility of combining the enhancement-mode FD/SOI NMOS with the AM/SOI PMOS to obtain almost symmetrical threshold voltages when using only the single n^+ polysilicon gate [Fay95]. However, AM devices are less resistant to the two-dimensional effects [Fay95] because of the enhanced source/drain charge sharing, which results in increased subthreshold leakage current. The AM SOI devices therefore are unsuitable for deep-submicron digital applications.

For the thin-film FD/SOI MOSFET, our physical subthreshold model with afforded insights from the supporting MEDICI simulations provides the basis for studying the scaling limit determined by subthreshold conduction and current drive at device/circuit level. To be systematic, we examine two levels of film-body doping, while considering technology parameters such as the gate material and film/buried-oxide thickness to meet required performance specifications (The front-gate oxide thickness is set to 4.5 nm due to oxide reliability [Uwa93]). To begin, let us assume that the film is heavily doped ($\geq 1x10^{18}$ cm^{-3}) to reduce the

charge-sharing effect. The high doping concentration causes a decrease of carrier mobility (drive current) due to Coulomb scattering by ionized dopant atoms. It also means that the film body is not strongly FD, hence implying floating-body effects like the previously discussed subthreshold kink. The film thickness needs to be thinned down to maintain the FD condition. Use of ultra-thin film gives rise to high source/drain resistance, which degrades the drive current; novel techniques such as Ti/Co salicidation [Su94] and selective-epi technique [Hwan94] to improve the series resistance are needed. Good film uniformity is also necessary to reduce the threshold voltage variation, which is linearly proportional to the (high) film doping [Vee88], across the wafer. Ultimately the manufacturing problems will be the main constraints in preventing film thickness from being scaled below 20 nm.

Using low body doping ($\leq 5 \times 10^{17}$ cm^{-3}) and thicker film thickness ($\geq$ 50 nm) relaxes the manufacturing constraints, and suppresses the subthreshold kink. It however enhances the source/drain charge-sharing effect. In order to control the leakage current but maintain reasonable current drive, a mid-gap work-function material is considered for front gate electrode. The other option, discussed previously, is to scale the buried oxide with selective substrate implantations to minimize the two-dimensional effects.

We use SOI-SPICE to examine the viability of low body doping by simulating 0.1-μm CMOS devices and circuits with dual-poly and (mid-gap) TiN [Hwan92] gates. In this study, leakage current of 1.0 nA/μm, with threshold voltage of 0.2-

0.3 V, is targeted for 1.0 V technology. Fig. 5.16 shows the predicted CMOS subthreshold characteristics and inverter circuit performances for both types of gate materials operated at V_{DD} = 1.0 V. In the dual-poly-gate design, we use N_{body} = $5x10^{17}$ cm^{-3}, t_b = 50 nm, and t_{ob} = 50 nm with selectively implanted substrate (N_{sub} = $1x10^{18}$ cm^{-3}). As indicated in Fig. 5.16(a), the NMOS leakage resulting from using an n^+ poly gate is too high ($\approx$ 100 nA/μm) because of significant charge-sharing effects evidenced by the large S (100 mV/dec). If we scale down the film to inhibit these effects, we must increase the body doping for acceptable threshold voltage, and we hence return to the first case discussed above.

For the TiN-gate device, which has the same film thickness (50 nm) but thick buried oxide (350 nm), the body doping was adjusted (N_{body} = $3.8x10^{17}$ cm^{-3}) to achieve the same leakage as the dual-poly-gate NMOS for reasonable comparison. The resulting performance degradation on subthreshold slope (S = 200 mV) and high threshold (V_{TH} = 0.45 V) suggests poor performance for a 1-V power supply. These insights are illustrated by 4-stage CMOS inverter simulation results presented in Fig. 5.16(b). The widths of the n- and p-channel devices are 6.6 μm and 3.3 μm, respectively. The inverter using TiN is basically non-functional, which contrasts with the good performance (about 25 psec delay) achieved by using dual-poly gates with selective substrate implantation. However, the leakage-current problem needs to be resolved, which may have to rely on designing subthreshold current-reduction circuits.

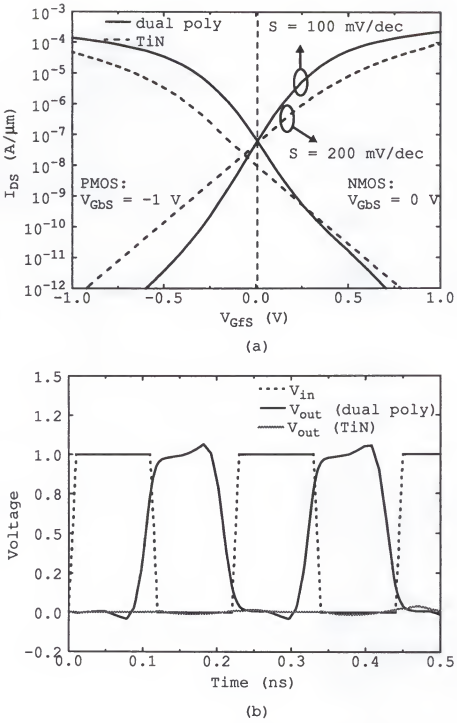


Fig. 5.16 SOI-SPICE-predicted (a) CMOS devices subthreshold characteristics and (b) inverter circuit performance using dual poly and TiN technologies. L = 0.1 μm, V_{DD} = 1.0 V.

5.5 Summary

A rigorous study of the design of deep-submicron FD/SOI low-voltage CMOS technology is done by device/circuit simulations using SOI-SPICE. Design tradeoffs involving speed performance and standby power consumption in scaled, deep-submicron SOI CMOS technology were revealed. The simulations suggest that the advantages of the conventional FD/SOI structure vanish as the device channel length is scaled to the 0.1-μm regime. The reason is mainly due to the two-dimensional field in the thin film and the buried oxide, which increases the leakage current. The subthreshold kink effect and back-gate depletion effect further limit design optimization for scaled FD/SOI. In light of the apparent show-stopping features of conventional scaled FD/SOI CMOS for highly scaled digital circuits, a substantial technological advance would seem to be required to salvage FD/SOI.

CHAPTER 6
DUAL-GATE FULLY DEPLETED SOI: A PROMISING TECHNOLOGY FOR FUTURE DIGITAL APPLICATIONS

6.1 Introduction

The insight gained from our previous studies suggest that the conventional (i.e., single-gate) FD/SOI technology cannot be scaled for future ULSI CMOS applications due to fundamental source/drain charge-sharing and fringing-field effects on threshold voltage and leakage current. Control of these effects for sub-0.2μm technology would require prohibitively thin SOI film and high channel doping. Thinning the back oxide tends to ameliorate the effects, but substrate depletion effects undermine the benefit of such scaling.

To overcome the scaling barrier implied for the FD/SOI technology then, a novel device structure such as the dual-gate (DG) thin-film FD/SOI MOSFET [Bal87], [Tan91], [Yan92], in which the electrical characteristics are controlled by "active" front and back gate voltages (instead of a grounded substrate in the conventional single-gate (SG) SOI device), is of interest. Fig. 6.1 shows a schematic cross-sectional view of an n-channel n^+-n^+ DG FD/SOI MOSFET, which has n^+ poly front and back gates. When compared to the conventional FD/SOI device shown in Fig. 1.1, we see that the buried oxide is replaced by a thermally grown oxide, and the original

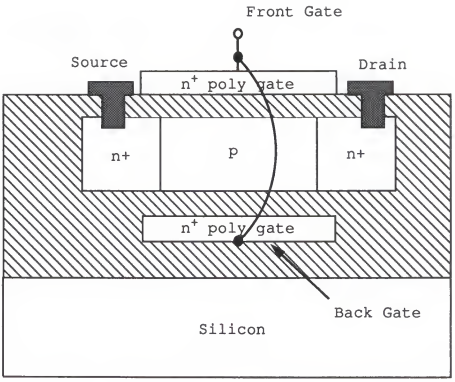


Fig. 6.1 A cross-sectional view of n-channel n^+-n^+ DG FD/SOI MOSFET. The back gate is externally tied to the front gate to yield most performance, as will be discussed later.

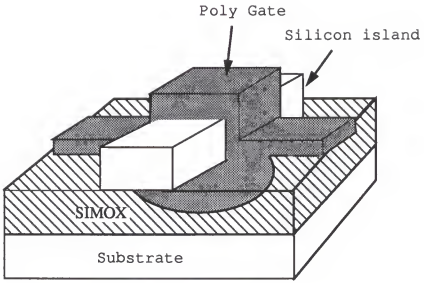
common p^- substrate is replaced by n^+ polysilicon to create a completely isolated second gate. The thin back gate oxide essentially eliminates the field fringing at the back surface. The unique "dual-channel" operation afforded by equal front and back gate voltages further reduces the source/drain charge-sharing effect and enhances the drive current as well. Experimental data also reveal that the subthreshold kink effect [Kri95], which impacts the design optimization as noted in Chapter 5, can be suppressed by the enhanced back-channel control [Tan94]. Furthermore, if the back gate can be well aligned with the channel, the circuit performance can be improved via elimination of the source/drain capacitance.

The objective of this chapter is to study the effect of second gate on device performance, and to conduct a preliminary design for sub-0.1μm DG FD/SOI CMOS based on SOI-SPICE simulations. In Section 6.2, a brief overview of proposed fabrication processes for DG FD/SOI MOSFETs is given. The advantages and disadvantages associated with each process are discussed as well. A qualitative discussion of the physics underlying superior DC performance of the DG device is presented in Section 6.3. SOI-SPICE simulations can be used to aid the discussion because it physically accounts for the weak-inversion diffusion of carriers at both the front and back surfaces as well as throughout the SOI film. Such accounting obviously is essential for modeling the subthreshold characteristics of the DG FD/SOI MOSFET. Since our model does not account for the above-threshold back-channel conduction, only a qualitative

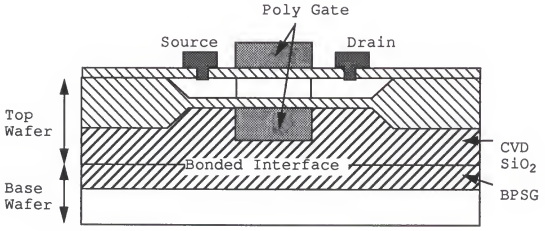
analysis of the speed performance is given; the primary focus is on the subthreshold characteristics, which implies whether off-state current and threshold voltage can be controlled, as well as whether the DG technology is scalable. The gained physical insight is then utilized in Section 6.4 to suggest a sub-0.1μm DG FD/SOI CMOS design. The projected performance is compared with that of conventional FD/SOI MOSFET with ultra deep-submicron (0.05 μm) channel length.

6.2 DG FD/SOI MOSFET Fabrication

Obviously the main technology challenge in realizing the DG device is forming the thin back-gate oxide (< 20 nm), which can not be done reliably on SIMOX material. Various approaches have been proposed to resolve this problem however. Colinge et al. proposed a "Gate-All-Around" structure [Col90] where the (single) polysilicon gate is formed on the top, the sides, and the bottom of the active film as shown in Fig. 6.2(a). In this process, a cavity is first created under the active region of the SOI island with buffered hydrofluoric acid (BHF). Thermal oxidation is then done to cover all the exposed silicon film, after which the polysilicon is deposited using low-pressure chemical vapor deposition (LPCVD). The polysilicon is heavily doped after the threshold voltage adjustment, but before the source/drain implantation step. The process is compatible with standard SOI processing, adding one additional mask and etching step, but is limited to the devices of relatively



(a)



(b)

Fig. 6.2 Schematic representations of (a) GAA and (b) bonding wafer DG FD/SOI MOSFETs.

large dimensions (e.g., L = 3 μm in [Col90]) due to needed isotropic etching. Furthermore, since only one (all-around) gate is formed, there is no flexibility for utilizing different gate materials or gate voltages to optimize the performance for different circuit applications.

Another process for fabricating deep-submicron DG thin-film SOI devices is wafer-bonding with etch-back [Tan91] as illustrated in Fig. 6.2(b). In this process, a field oxide is first grown over the (top) silicon wafer, and then a poly gate is formed, followed by SiO_2 deposition and planarization by polishing. A borophosphosilicate glass (BPSG) film is deposited on the base wafer, and the two wafers are then bonded using CVD SiO_2. After annealing, which strengthens the wafer bonding, the silicon layer which used to be the substrate of the top wafer is thinned down by chemical-mechanical polishing (CMP). Then front-gate formation, source/drain implantations, and the other key fabrication steps follow.

Recently, Denton et al. fabricated a p-channel DG FD/SOI MOSFET using silicon epitaxial growth (SEG) and epitaxial lateral overgrowth (ELO) techniques [Den95]. The process starts with an n-type silicon wafer, and a reactive ion-etching (RIE) back-gate trench is followed by oxidation, poly gate formation, and CMP. The wafer is then oxidized and patterned to define the active area of device. The exposed poly-gate is covered by the thermally grown oxide. SEG/LEO is grown out of the seed window defined next to the active area. The excess ELO is removed by CMP. Then front-gate formation, source/drain implantations, and the other key

fabrication steps follow. The ultimate device structure is illustrated in Fig. 6.3.

Both wafer bonding and SEG/ELO techniques enable optimization of device performance via different gate materials, and they are compatible with the conventional deep-submicron processing. Their main disadvantage is the low throughput with regard to IC production, which increases the product cost eventually.

6.3 Examination of DG FD/SOI Performance

In this section we study the performance of the DG FD/SOI MOSFET in terms of short-channel effect immunity and threshold voltage controllability using our developed physical subthreshold model in SOI-SPICE. The simulated devices in this study are presumably fabricated by a process which produces separate front and back gates, hence allowing different materials and biases. The key device parameters assumed are SOI film thickness of 30 nm, channel doping of 2×10^{17} cm^{-3}, which ensures the FD condition even for the long-channel (0.5 μm) device, and (front and back) oxide thickness of 4.5 nm. Both channel length (L) and film thickness (t_b) will be varied to gain physical insights and suggest design concepts regarding scaled DG FD/SOI CMOS.

6.3.1 Short-Channel Effect Immunity

We first compare the influence of the short-channel effect on both conventional single-gate (SG) and DG FD/SOI

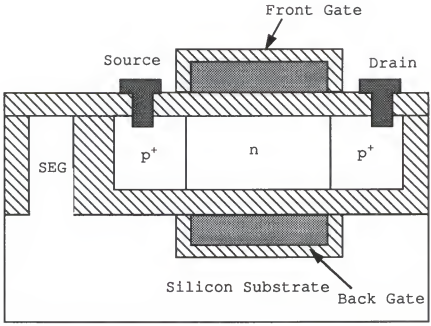


Fig. 6.3 A p-channel DG FD/SOI MOSFET using ELO/SEG technique.

MOSFETs. The SG device has a BOX thickness of 50 nm on a highly doped grounded substrate, which in fact yields best-case SG results because of the lack of substrate depletion that exacerbated the short-channel effects. The gate is n^+ polysilicon, which is also initially assumed for both gates of the DG device. Fig. 6.4 plots the SOI-SPICE-predicted subthreshold swing (S) of both devices at low drain bias (V_{DS} = 50 mV) versus L. Note first that even for long L, S (= 60 mV) of the DG device is less than that of the SG device. This superiority is due to the charge coupling [Lim85] influenced by the simultaneous biasing of the front and back gates; the threshold voltage decreases as the surface becomes inverted. Both SG and DG devices maintain the long-channel behavior with L scaled down to 0.15 μm. As L is shrunk to 0.1 μm and below however, the simulation results show that the DG devices exhibit far more superior short-channel-effect immunity than the SG device; for L = 0.075 μm, the S (76 mV) of the n^+-n^+ DG device is about one-half that of the SG device, whereas for L = 0.05 μm, the comparison is prohibitive.

The DG device superiority illustrated in Fig. 6.4 is due mainly to elimination of the BOX field fringing afforded by the thin (back) oxide in the DG device, complemented by the noted charge-coupling benefit from the simultaneous gate biasing. Indeed the severe deterioration of S of the SG device is due to back-surface inversion caused by the BOX field fringing, which is not controlled well by the (front) gate bias, V_{GfS}. In addition, it can also be attributed to the reduced source/drain charge-sharing variation with gate

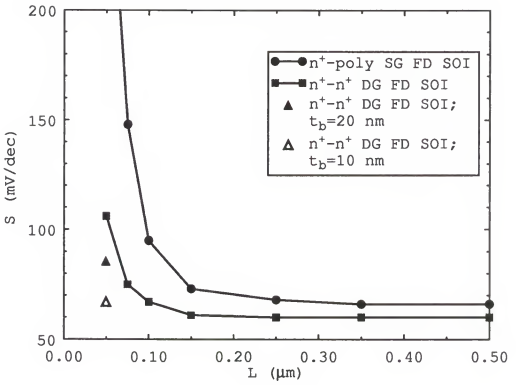


Fig. 6.4 SOI-SPICE-predicted subthreshold swing (S) as a function of channel length for the n^+-poly SG and n^+-n^+ DG FD/SOI MOSFETs; the triangle symbols represent the S of n^+-n^+ DG device at t_b = 20 nm and 10 nm; $N_A = 2 \times 10^{17}$ cm^{-3}, V_{DS} = 50 mV.

voltage following from the increased channel control. For example, Fig. 6.5 plots the predicted I_{DS}-V_{GfS} characteristics of the n^+-poly SG and n^+-n^+ DG FD/SOI MOSFETs with a channel length of 0.1 μm. For the SG device, it reflects that as V_{GfS} is increased in the weak-inversion region, the vertical electric field becomes more predominant, reflecting less two-dimensionality (i.e., less charge sharing by source and drain), and hence the threshold voltage increases, which results in lower $\log(I_{DS})$-V_{GfS} slope. For the DG device, the field tends to be predominantly vertical for all V_{GfS}, and hence the source/drain charge sharing is small and the subthreshold slope is high relative to the SG device.

Any source/drain charge-sharing effect in the sub-0.1μm n^+-n^+ DG device can be further ameliorated by continuously scaling down the film thickness. The S predictions for t_b = 20 and 10 nm in Fig. 6.4 show that for L = 0.05 μm, S decreases from 107 mV to 66 mV as t_b is thinned from 30 nm to 10 nm. Obviously the best characteristics attainable will simply depend on the thinnest SOI film that can be realized from the technology.

6.3.2 Threshold Voltage Controllability

Although the n^+-n^+ DG FD/SOI MOSFET exhibits excellent short-channel effects immunity, its threshold voltage, as reflected by Fig. 6.5, is too low because of the front gate-back gate charge coupling. In fact, it is negative as shown in Fig. 6.6 where SOI-SPICE predictions of threshold

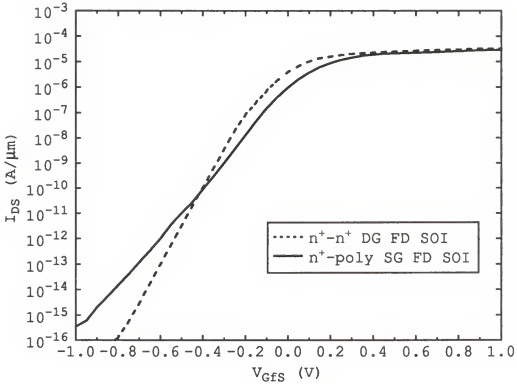


Fig. 6.5 SOI-SPICE simulated I_{DS} - V_{GfS} characteristics of n-channel n^+ poly SG and n^+-n^+ DG FD/SOI MOSFETs; L = 0.1 μm, V_{DS} = 50 mV.

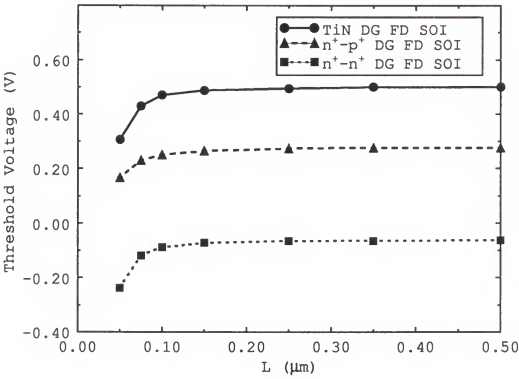


Fig. 6.6 SOI-SPICE-predicted threshold voltage versus channel length for TiN-TiN, n^+-p^+, and n^+-n^+ DG FD/SOI MOSFETs; $N_A = 2 \times 10^{17}$ cm^{-3}, $t_b = 30$ nm, and $V_{DS} = 50$ mV.

voltages versus channel length are plotted. (We extracted the threshold as the value of V_{GS} required for I_{DS} = 0.1 x W/L (μA) at V_{DS} = 50 mV.) Increasing N_A would yield higher threshold voltage, but would necessitate thinner t_b. We must therefore consider different gate material to increase the flatband voltage, and allow for asymmetrical gates for ultimate control of threshold voltage. We consider a mid-gap material such as TiN [Suz95] for a symmetrical device, and n^+ polysilicon for the front gate and p^+ polysilicon for the back for an asymmetrical device. (The use of p^+ polysilicon for both gates is not considered because of the implied high threshold voltage.) SOI-SPICE-predicted threshold voltage versus L for these two variations of the DG device are included in Fig. 6.6. Note that the threshold voltage for the symmetric TiN-gate device is probably too high for sub-0.1μm applications for which the supply voltage will be less than 1 V. Decreasing N_A would lower the threshold voltage, but would also exacerbate the short-channel effects. Only the asymmetrical n^+-p^+ DG FD/SOI MOSFET shows acceptable threshold voltage (about 0.3 V for $N_A = 2 \times 10^{17}$ cm^{-3}), which could be further adjusted by tuning N_A.

Notice also in Fig 6.6 that the n^+-p^+ DG device shows the least roll-off of threshold voltage with decreasing L. Physical insight from our simulations reveals that this superiority of the asymmetrical device is related to the distribution of weak-inversion channel current in the SOI film. The predominant current flows (by diffusion) at the front surface, in contrast to the symmetrical devices in which the predominant current is due to electron diffusion

in the center of the film, which is less controlled by the gates. To illustrate this insight, we plot in Fig. 6.7 the variation of electrostatic potential across the SOI film at the center of the channel in both the n^+-n^+ and n^+-p^+ DG devices for several subthreshold gate voltages. The potential variation, which we have corroborated by numerical (MEDICI) device simulations, is part of the two-dimensional analytic solution that underlies the subthreshold FD/SOI MOSFET model in Chapter 3. Note the maximum of the potential at the center of the film in the symmetrical device, which reflects the peak electron density and current. In fact this internal maximum is a ramification of the charge sharing in the short-L device. As V_{GS} is increased, the vertical field becomes more significant, and the surface potentials increase more than the internal potential, ultimately, in strong inversion, forming the more familiar U-shaped potential across the film [Lim85]. Hence, the inferior short-channel effect immunity of the symmetrical DG FD/SOI MOSFETs reflects a form of punchthrough current, which does not flow in the asymmetric device.

Fig. 6.8 plots the SOI-SPICE-predicted threshold voltage of 0.1-μm devices for different film thickness. We see that the threshold voltage of the n^+-p^+ DG device is actually increased as we scale down t_b. This undesirable sensitivity might be explained by the suppressed source/drain charge-sharing effect. This is not true though because the simulated device has an almost ideal S (68 mV) for the thick 50-nm film already. In fact, the increased threshold voltage is caused by the increased gate coupling. As the film

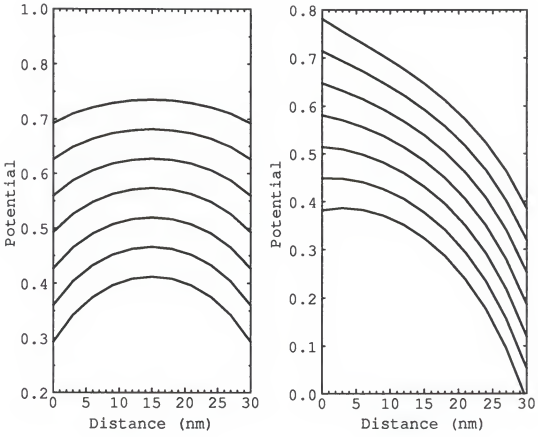


Fig. 6.7 Calculated potential distribution in the film for (a) n^+-n^+ and (b) n^+-p^+ DG FD/SOI MOSFETs. The increasing potentials correspond to V_{GS} increasing from -0.6 V to 1.0 V in 0.1 V step; L = 0.05 μm, t_b = 20 nm, $N_A = 2 \times 10^{17}$ cm^{-3}, and V_{DS} = 50 mV.

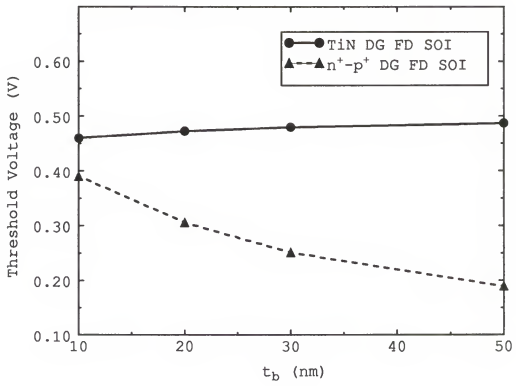


Fig. 6.8 SOI-SPICE-predicted threshold voltage versus film thickness for TiN-TiN and n^+-p^+ DG FD/SOI MOSFETs; L = 0.1 μm; V_{DS} = 50 mV.

is thinned down, the front gate has to support the back-surface field, which terminates at the back gate instead of the surface due to positive flatband voltage, through charge coupling; hence the front surface becomes less depleted, resulting in an increase of threshold voltage. This coupling mechanism actually overwhelms the reduced body-charge effect on the threshold voltage, which is linearly proportional to the film thickness [see Eq.(3.35)]. For the TiN-TiN DG FD/SOI, the threshold voltage determined by the work function is essentially insensitive to the t_b variation.

6.3.3 Current Drive

Another important advantage of dual-gate operation is the enhanced current drive, in particular for the symmetrical n^+-n^+ and TiN-TiN DG FD/SOI MOSFETs. Specifically, two-times enhancement in drain current afforded by the second channel was reported for the n^+-n^+ DG devices at constant effective gate voltage, $V_G - V_{TH}$, when compared to the conventional SG device [Ven92]. The afforded speed improvement can be compromised however, especially in a circuit whose load capacitance is dominated by the gate capacitance. To get the most benefit, the device should be operated in moderate inversion, or slightly above threshold, where the volume inversion prevails. The volume inversion provides enhancement on the drive current and transconductance due to lower scattering rate (i.e., higher mobility) in the body, which is beneficial in high-performance/low-power analog applications.

For the asymmetrical n^+-p^+ DG FD/SOI MOSFET, the second channel is forfeited due to the use of p^+ poly gate. However the simultaneous front gate/back gate biasing can still boost the front current in the strong inversion by charge coupling when compared to the conventional SG FD/SOI MOSFET.

6.4 Preliminary Sub-0.1μm DG FD/SOI CMOS Design

In this section we study the 0.05-μm DG FD/SOI CMOS design with SOI-SPICE to assess aggressive scaling. The design criteria include obtaining reasonable leakage current (1 nA/μm) and steep subthreshold slope at the supply voltage of 1.0 V, which results in higher saturation current. (We stress however that this design study is not optimal nor complete. For example, the back-channel current in the strong-inversion region is not accounted for in our model, which, obviously for the symmetrical DG device, can be significant.)

The threshold voltage of the n^+-n^+ DG device is too low to suppress the leakage current (see Fig. 6.6), and can hardly be adjusted by simply increasing the film doping. Using TiN for both gates increases the threshold voltage though, but the value (0.4 ~ 0.5 V) seems to be too high for the supply voltage of 1.0 V. Our design therefore presumes the asymmetric n^+-p^+ DG structure due to its better threshold voltage scalability and short-channel behavior. The additional back gate biasing further improves the current drive when compared to the conventional SG device.

As illustrated in Fig 6.4 for a sub-0.1μm device, ultra-thin film is required to reduce the source/drain charge-sharing effect while maintaining low body doping in order to limit the mobility degradation and subthreshold kink. The predicted I_{DS}-V_{Gfs} characteristics in Fig. 6.9 show that with the channel doping density of $4x10^{17}$ cm^{-3}, the film thickness of the n^+-p^+ DG device needs to be thinned down to 15 nm in order to achieve steep slope (67 mV) and reasonable leakage. When compared to the SG device realized here by grounding the back gate of the DG device, the n-channel DG device exhibits significant improvement in S and current drive due to enhanced back-channel controllability and front-gate/back-gate charge coupling. For the p-channel device, the simulation results in Fig. 6.9 show significant leakage-current reduction is obtained in dual-gate operation, mainly because the $-V_{DD}$ back gate bias is eliminated.

6.5 Summary

The viability of dual gate FD/SOI for high-performance/low-power digital applications was studied at the device level by SOI-SPICE simulations. We showed that the DG FD/SOI MOSFET is able to extend the scaling limitation of FD/SOI technology beyond the 0.1-μm regime due to superior short-channel immunity. We studied the performance of the DG FD/SOI device using different gate materials. The study revealed that using standard n^+ polysilicon for both gates does not improve the leakage current due to the low threshold

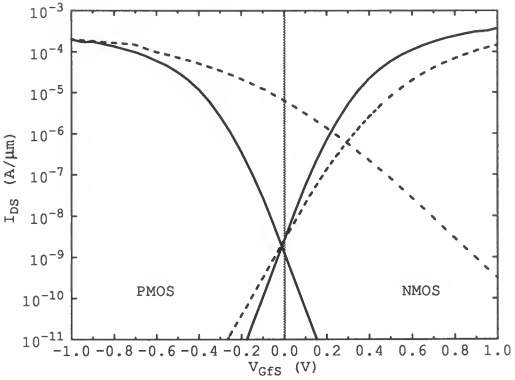


Fig. 6.9 SOI-SPICE-predicted I_{DS}-V_{GfS} characteristics of n^+-p^+ DG (solid curves) and n^+-poly SG (dashed curves) CMOS devices; L = 0.05 μm, t_b = 15 nm, and V_{DS} = 1.0 V.

voltage. Use of mid-gap TiN increases the threshold voltage, but it seems to be too high for 1.0 V circuit operation. The n^+-p^+ DG device is most attractive for sub-0.1μm low-voltage applications because of better short-channel effects immunity and scalable threshold voltage. Even though the second channel is forfeited by increasing the back-channel threshold voltage, a good enhancement on drive current can be obtained from the increased back gate biasing when the device is driven into the strong-inversion region.

Finally we suggest that a more thorough study of the DG FD/SOI MOSFET device/circuit performance versus different gate material and/or front-gate/back-gate voltage is necessary, and that SOI-SPICE, upgraded with strong-inversion back-channel current modeling, can be a efficient tool for predictive device/circuit simulations in this regard.

CHAPTER 7
SUMMARY AND SUGGESTIONS FOR FUTURE WORK

In this dissertation, physical modeling and comprehensive design studies of scaled FD/SOI CMOS for low-voltage/power circuit applications were presented. The main contributions and conclusions of the research are summarized as follows.

In Chapter 2, effects of the parasitic BJT in the floating-body FD/SOI MOSFET and its unique repercussions in the scaled technology were studied at the circuit level under DC and transient conditions. The studies revealed that the bipolar problem, which translates to loss of gate control, overwhelms the benefit, and hence must be alleviated through design tradeoffs. Results of extensive SOI-SPICE circuit simulations indicated the efficacy of optimized LDD/LDS structure in suppressing the BJT-induced problems, while maintaining superior performance over bulk-silicon CMOS. (Benchmark studies revealed that speed superiority of SOI, especially for scaled supply voltage, is mainly due to the enhanced drive current as well as the reduced parasitic (junction) capacitance.)

In Chapter 3, results of two-dimensional numerical device simulations showed that the viability of thin-film FD/SOI is threatened by significant short-channel effects in the subthreshold region as the channel length is scaled to the deep-submicron regime. The physical insight attained was

used to aid the development of a physical MOSFET model essential for deep-submicron low-voltage FD/SOI circuit simulation and design. The subthreshold model accounts for two-dimensional source/drain charge sharing in the SOI film body and fringing fields from the source and drain junctions in the underlying (back) oxide (BOX). It further accounts for the diffusion of carriers throughout the thin-film body, which is supplemented with the related charge modeling. A cubic polynomial interpolation is used to link the weak- and strong-inversion currents based on physically defined moderate-inversion boundaries, between which the model charges are interpolated as well.

In Chapter 4, the implementation of the new FD/SOI MOSFET model into SOI-SPICE (Ver. 4.1) was described in detail. An efficient parameter-evaluation algorithm was defined based on the device structure, facilitating model verification. The subthreshold model was verified by comparison with numerical device simulations and measurements of test devices with varying dimensions; the model was shown to be predictive for deep-submicron devices without requiring substantive empirical fitting.

In Chapter 5, the utility of SOI-SPICE was demonstrated at device and circuit levels by using it in FD/SOI CMOS design studies based on speed and static power consumption. Results of a preliminary study suggest that the performance of conventional (single-gate, dual-poly) FD/SOI is attractive for quarter-micron digital CMOS applications, but may not be adequate for the < 0.2-μm regime due to excessive leakage currents caused by the short-channel effects. It was

found that use of thin BOX can control the field fringing, but tends to produce excessive leakage current in the PMOS device because of enhanced back-gate coupling. Design alternatives (for example, n^+ poly gates or hybrid FD/PD designs) were suggested, showing improved power consumption but involving tradeoffs. However, as channel length approaches 0.1 μm, it was shown that the short-channel effects in FD/SOI MOSFETs cannot be controlled, even with major technology changes, for example, mid-gap gates or selectively implanted substrate), and that the subthreshold kink and back-gate depletion effects further limit design optimization. In light of the apparent show-stopping features of conventional scaled FD/SOI, technology innovation seems to be needed.

In Chapter 6, performance of a novel dual-gate (DG) thin-film FD/SOI structure, which in principle has features called for in the design study of Chapter 5, was studied at the device level using SOI-SPICE. It was shown that DG FD/SOI MOSFET can extend the scaling limitation of FD/SOI technology beyond the 0.1-μm regime because of superior short-channel effect immunity. The simulations suggested that an asymmetrical n^+-p^+ DG FD/SOI MOSFET is most promising for sub-0.1μm low-voltage applications due to better threshold-voltage control. Although the second channel is forfeited in this design, the charge coupling and the simultaneous front gate-back gate biasing can still boost the front-channel current in strong inversion significantly above that of the single-gate device. An undesirable sensitivity problem of threshold voltage of the asymmetrical

device ultimately will require improvement of the SOI film uniformity however.

The following tasks are suggested as future works to improve the robustness of the SOI-SPICE circuit simulator for future applications.

(1) Model enhancement for the strong-inversion current and charge. Our current moderate-inversion modeling may be inadequate due to inconsistencies in the weak- and strong-inversion analyses. Whereas the two-dimensional analysis done in weak inversion is physical, that in strong inversion, based on geometrical body charge partitioning among the gates, source, and drain, is inadequate. This inconsistency can result in non-physical characterization of current and charges in the moderate-inversion region, which possibly underlies simulation errors and convergence problems.

(2) Improvement of the current and charge transition from subthreshold to the strong-inversion region. The cubic (for current) and linear (for charge) polynomial interpolations discussed in Chapter 3 are too complex and simple, respectively, and may result in abnormal conductance as well as capacitance, rendering SOI-SPICE inadequate for simulating analog circuits. A more compact yet accurate current expression may be realized by accounting for different degrees of drift and diffusion current components in moderate inversion. A similar approach can be applied to the moderate-inversion charge calculation as well. Work on smoothing the current transition from linear to the

saturation region (now involving an abrupt velocity saturation) should be also included in this task.

(3) Extension of SOI-SPICE for simulating DG FD/SOI MOSFETs. The study presented in Chapter 6 demonstrates the superior short-channel immunity and scaling capability afforded by the dual-gate FD/SOI structure. It however implies the need for strong-inversion modeling for the back-channel conduction in order to generally evaluate symmetrical DG FD/SOI circuit performance relative to that of the asymmetrical design proposed.

(4) Assessment of FD/SOI analog circuit applications. Although the leakage issue plagues the deep-submicron FD/SOI digital applications, it has less impact on the analog circuit applications. Because of the enhanced current drive and reduced source/drain capacitances, a properly designed FD/SOI analog circuit can outperform bulk-silicon counterparts, especially in low-voltage applications. In addition, FD/SOI is also superior to PD/SOI in analog applications due to fewer (DC and dynamic) floating-body effects. These potential advantages reinforce the need for more sophisticated moderate-inversion analysis (see (2)) in the SOI-SPICE FD model for reliable analog circuit simulation. Model enhancements such as self-heating and noise effects should be also included in this task.

REFERENCES

[All93] M. Alles and W. Krull, "Considerations for SIMOX Low Voltage Applications," Proc. 1993 IEEE Internat. SOI Conf., pp. 102-103, Palm Springs, CA, Oct. 1993.

[Bal87] F. Balestra, S. Cristoloveanu, M. Benachir, and T. Elewa "Double-Gate SILICON-ON-INSULATOR with Volume Inversion," IEEE Electron Devices Lett., vol. EDL-8, pp. 410-412, 1987.

[Cha87] P. C. Chan, R. Liu, S. K. Lau, and M. Pinto-Guedes, "A Subthreshold Conduction Model for Circuit Simulation of Submicron MOSFET," IEEE Trans. on CAD, vol. CAD-6, pp. 574-581, July 1987.

[Che92] H. -S. Chen and S. S. Li, "A Model for Analyzing the Interface Properties of a Semiconductor-Insulator-Semiconductor Structure-I: Capacitance and Conductance Techniques," IEEE Trans. Electron Devices, vol. 39, pp. 1740-1746, July 1992.

[Cho91] J. Y. Choi, "Modeling and simulation of the fully depleted silicon-on-insulator MOSFET for submicron CMOS IC design," Ph.D. dissertation, University of Florida, Gainesville, 1991.

[Col90] J. -P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, "Silicon-On-Insulator "Gate-All-Aroubd Device,"" Tech. Digest International Electron Device Meet., pp. 595-598, Dec. 1990.

[Col91] J. -P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI. Boston, MA: Kluwer, 1991.

[Den95] J. P. Denton and G. W. Neudeck, "Fully Depleted Dual-Gate Thin-Film SOI P-MOSFET with an Isolated Buried Polysilicon Backgate," Proc. 1995 IEEE Internat. SOI Conf., pp. 135-136, Tucson, AZ, Oct. 1995.

[Fay95] O. Faynot, "Charactèrisation et Modèlisation du Fonctionnement des Transistor MOS Ultra-Submicroniques Fabriques sur films SIMOX Trés Minces," Ph.D. dissertation, l'Institute National Polytechnique de Grenoble, October 1995.

[Fos92] J. G. Fossum, SOISPICE-2 User's Manual, University of Florida, Gainesville, FL, Feb. 1992.

[Fos93] J. G. Fossum, P. C. Yeh, and J. -Y. Choi, "Computer-Aided Performance Assessment of Fully Depleted SOI CMOS VLSI Circuits," IEEE Trans. Electron Devices, vol. 40, pp. 598-604, March 1993.

[Fos95] J. G. Fossum, SOI-SPICE-4 User's Manual, University of Florida, Gainesville, FL, March 1995.

[Guo93] J. -Y. Guo and C. -Y. Wu, "A New 2D Analytic Threshold-Voltage Model for Fully Depleted Short-Channel SOI MOSFET's," IEEE Trans. Electron Devices, vol. 40, pp. 1653-1661, Sept. 1993.

[Hwa93] B. -Y. Hwang, J. Tsao, M. Racanelli, M. Huang. J. Foerstner, T. Wetteroth, and I. -S. Lim, "Design and Manufacturing Considerations of a 0.5 µm CMOS Technology on TFSOI," Proc. International SOI Conference, pp.128-129, Palm Springs, CA, Oct. 1993

[Hwan92] J.-M. Hwang and G. P. Pollack, "New gate electrodes for fully-depleted SOI/CMOS; TiN and POLY Si-Ge," Proc. International SOI Conference, pp.148-149, Ponte Vedra Beach, FL, Oct. 1992

[Hwan93] J.-M. Hwang, E. Yee, T. Houston, and G. P. Pollack, "High performance submicron SOI/CMOS with an elevated source/drain structure," Proc. International SOI Conference, pp.132-133, Palm Springs, CA, Oct. 1993

[Joa95] H. -O. Joachim, Y. Yamaguchi, Y. Inoue and T. Hirao, "Comparison of Standard and Low-Dose SIMOX Substrates for 0.15µm SOI MOSFET Applications," Ext. Abst. Solid State Device Meet., pp. 854-856, Osaka, Japan, June 1995.

[Kad95] Y. Kado, H. Inokawa, Y. Okazaki, T. Tsuchiya, Y. Kawai, M. Sato, Y.Sakakibara, S. Nakayama, H. Yamada, M. Kitamura, S. Nakashima, K. Nishimura, S. Date, M. Ino, K. Takeya, and T. Sakai, "Substantial Advantages of Fully-Depleted CMOS/SIMOX Devices as Low-Power High-Performance VLSI Components Compared with its Bulk-CMOS Counterpart," Tech. Digest International Electron Device Meet., pp. 635-638, Dec. 1995.

[Kri93] S. Krishnan and J. G. Fossum, "Non-Local Modeling of Impact Ionization for Optimal Device/Circuit Design in Fully Depleted SOI CMOS Technology," Proc. 1993 IEEE International SOI Conf., pp. 114-115, Palm Springs, CA, Oct. 1993.

[Kri95] S. Krishnan, J. G. Fossum, P. C. Yeh, O. Faynot, S. Cristoloveanu, and J. Gauiter, "Floating-Body Kinks and Dynamic Effects in Fully Depleted SOI MOSFETs," Proc. 1995 IEEE International SOI Conf., pp. 10-11, Tucson, AZ, Oct. 1995.

[Lim85] H. K. Lim and J. G. Fossum, "A Charge-Based Large-Signal Model for Thin-Film SOI MOSFETs," IEEE Trans. Electron Devices, vol.ED-32, pp. 446-454, Feb. 1985.

[MED92] MEDICI User's Manual, Technology Modeling Associates Inc., Palo Alto, CA, 1992

[Mul86] R. S. Muller and T. I. Kinins, Device Electronics for Integrated Circuits, 2nd ed. New York: Wiley, 1986.

[Nag75] L. W. Nagel, "SPICE2: A computer program to simulate semiconductor circuits," Electronic Research Lab., University of California, Berkelay, ERL Memo ERL-M520, May 1975.

[Omu93] Y. Omura, S. Nakashima, K. Izumi, and T. Ishii, "0.1-μm-Gate, Ultrathin-Film CMOS Devices using SIMOX Substrate with 80-nm-Thick Buried Oxide Layer," IEEE Trans. Electron Devices, vol. 40, no. 5, pp. 1019-1022, Feb. 1985.

[Sha93] G. G. Shahidi, T. H. Ning, T. I. Chappell, J. H. Comfort, B. A. Chappell, R. Franch, C. J. Anderson, P. W. Cook, S. E. Schuster, M. G. Rosenfield, M. R. Polcari, R. H. Dennard, and B. Davari, "SOI for a 1-volt CMOS technology and application to a 512Kb SRAM with 3.5ns access time," Tech. Digest International Electron Device Meet., pp. 813-816, Dec. 1993

[Shah93] G. G. Shahidi, B. Davari, T. J. Bucelot, P. A. Ronsheim, P. J. Coane, S. Pollack, C. R. Blair, B. Clark, and H. H. Hansen, "Indium channel implant for improved short-channel behavior of submicrometer NMOSFET's," IEEE Electron Devices Lett., vol.14, No. 8, pp. 409-411, August 1993.

[Sme93] P. Smeys, U. Magnusson, and J. P. Colinge, "Non-destructive characterization of SOI wafers using spectroscopic reflectometry," Solid-State Electron., vol. 36, pp. 1213-1216, 1993.

[Slo91] J. W. Slotboom, G. Streutker, M. J. v. Dort, P. H. Woerlee, A. Pruijmboom, and D. J. Gravesteijn, "Non-Local Impact Ionization in Silicon Devices," Tech. Digest International Electron Device Meet., pp. 127-130, Dec. 1991.

[Su93] L. T. Su, J. B. Jacobs, J. E. Chung, and D. A. Antoniadis, "Short-Channel Effects in Deep-Submicrometer SOI MOSFETs," Proc. International SOI Conference, pp.112-113, Palm Springs, CA, Oct. 1993

[Suh95] D. Suh and J. G. Fossum, "A physical charge-based model for non-fully depleted SOI MOSFET's and its use in assessing floating-body effects in SOI CMOS circuits," IEEE Trans. Electron Devices, vol. 42, pp. 728-737, April 1995.

[Suz95] K. Suzuki and T. Sugii, "Analytical Models for n^+-p^+ Double-Gate SOI MOSFET's," IEEE Trans. Electron Devices, vol. 42, pp. 1940-1948, Nov. 1995.

[Sze81] S. M. Sze, Physics of Semiconductor Devices, 2nd Ed. Wiley: New York, NY, 1981.

[Tan91] T. Tanaka, H. Horie, S. Ando, and S. Hijiya, "Analysis of P^+ Poly Si Double-Gate Thin-Film SOI MOSFETs," Tech. Digest International Electron Device Meet., pp. 683-686, Dec. 1991.

[Tan94] T. Tanaka, K. Suzuki, H. Horie, and T. Sugii, "Ultrafast Operation of Vth-Adjusted p^+-n^+ Double-Gate SOI MOSFET's" IEEE Electron Devices Lett., vol.15, No. 10, pp. 386-388, October 1994.

[Tay78] G. W. Taylor, "Subthreshold Conduction in MOSFET's," IEEE Trans. Electron Devices, vol. ED-25, pp. 337-350, March 1978.

[Tma89] TMA-PISCES-2B: Two-Dimensional Device Analysis Program. Technology Modeling Assoc., Inc., Palo Alto, CA, 1989.

[Tma94] TMA-SUPREM-3: One-Dimensional Process Simulation Program. Technology Modeling Assoc., Inc., Palo Alto, CA, 1994.

[Tsi82] Y. Tsividis, "Moderate Inversion in MOS Devices," Solid-State Electron., vol. 25, pp. 1099-1104, 1982.

[Tsu94] T. Tsuchiya, T. Ohno, and Y. Kado, "Present Status and Potential of Subquarter-Micron Ultra-Thin-Film CMOS/SIMOX Technology," Proc. Sixth Internat. Symp. on SOI Technology and Devices, ECS vol. 94-11, pp. 401-412, May 1994.

[Uwa93] K. Uwasawa, T. Mogami, T. Kunio, and M. Fukuma, "Scaling Limitations of Gate Oxide in p^+ Polysilicon Gate MOS Structures for Sub-Quarter Micron CMOS Devices," Tech. Digest International Electron Device Meet., pp. 895-898, Dec. 1993.

[Vee88] S. Veeraraghavan and J. G. Fossum, "A Physical Short-Channel Model for the Thin-Film SOI MOSFET Applicable to Device and Circuit CAD," IEEE Trans. Electron Devices, vol. 35, pp. 1866-1875, Nov. 1988.

[Vee89] S. Veeraraghavan and J. G. Fossum, "Short-Channel Effects in SOI MOSFET's," IEEE Trans. Electron Devices, vol. ED-36, pp. 522-528, March 1989.

[Ven92] S. Venkatesan, G. W. Neudeck, and R. F. Pierret, "Dual-Gate Operation and Volume Inversion in n-Channel SOI MOSFET's," IEEE Electron Devices Lett., vol.13, No. 1, pp. 44-46, January 1992.

[Woe89] P. H. Woerlee, A. H. van Ommen, H. Lifka, C. A. H. Juffermans, L. Plaja, and F. M. Klaassen, "Half-Micron CMOS on Ultra-Thin Silicon on Insulator," Tech. Digest International Electron Device Meet., pp.821-824, Dec. 1989.

[Yan92] R. -H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From Bulk to SOI to Bulk," IEEE Trans. Electron Devices, vol. 39, pp. 1704-1710, July 1992.

[Yma89] T. Yamaguchi and T. H. Yuzuriha, "Process Integration and Device Performance of a Submicrometer BiCMOS with 16-GHz f_t Double Poly-Bipolar Devices," IEEE Trans. Electron Devices, vol. ED-36, pp. 890-896, May 1989.

[You89] K. K. Young, "Short-Channel Effects in Fully Depleted SOI MOSFET's," IEEE Trans. Electron Devices, vol. 36, pp. 399-402, Feb. 1989.

BIOGRAPHICAL SKETCH

Ping Chin Yeh was born in Taiwan, Republic of China, in 1965. He received the B.S. degree in 1987 from Tamkang University, Tamsui, Taiwan, and the M.S. degree in 1992 from the University of Florida, Gainesville, both in electrical engineering.

In 1992 he began pursuing the Ph.D. degree in electrical engineering at the University of Florida, Gainesville. His research interests are focused on compact device modeling for thin-film SOI MOSFETs as well as low-voltage circuit design. Upon graduation he will join Hewlett-Packard Company, in Palo Alto, California, as an IC Development Engineer working on SPICE/circuit simulation models for CMOS processes.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Jerry G. Fossum, Chairman
Professor of Electrical and
Computer Engineering

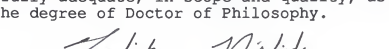
I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Robert M. Fox
Associate Professor of Electrical
and Computer Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Mark E. Law
Associate Professor of Electrical
and Computer Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.



Toshikazu Nishida
Associate Professor of Electrical
and Computer Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Chen-Chi Hsu
Professor of Aerospace Engineering,
Mechanics, and Engineering Science

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

May 1996

Winfred M. Phillips
Dean, College of Engineering

Karen A. Holbrook
Dean, Graduate School